Product Brief
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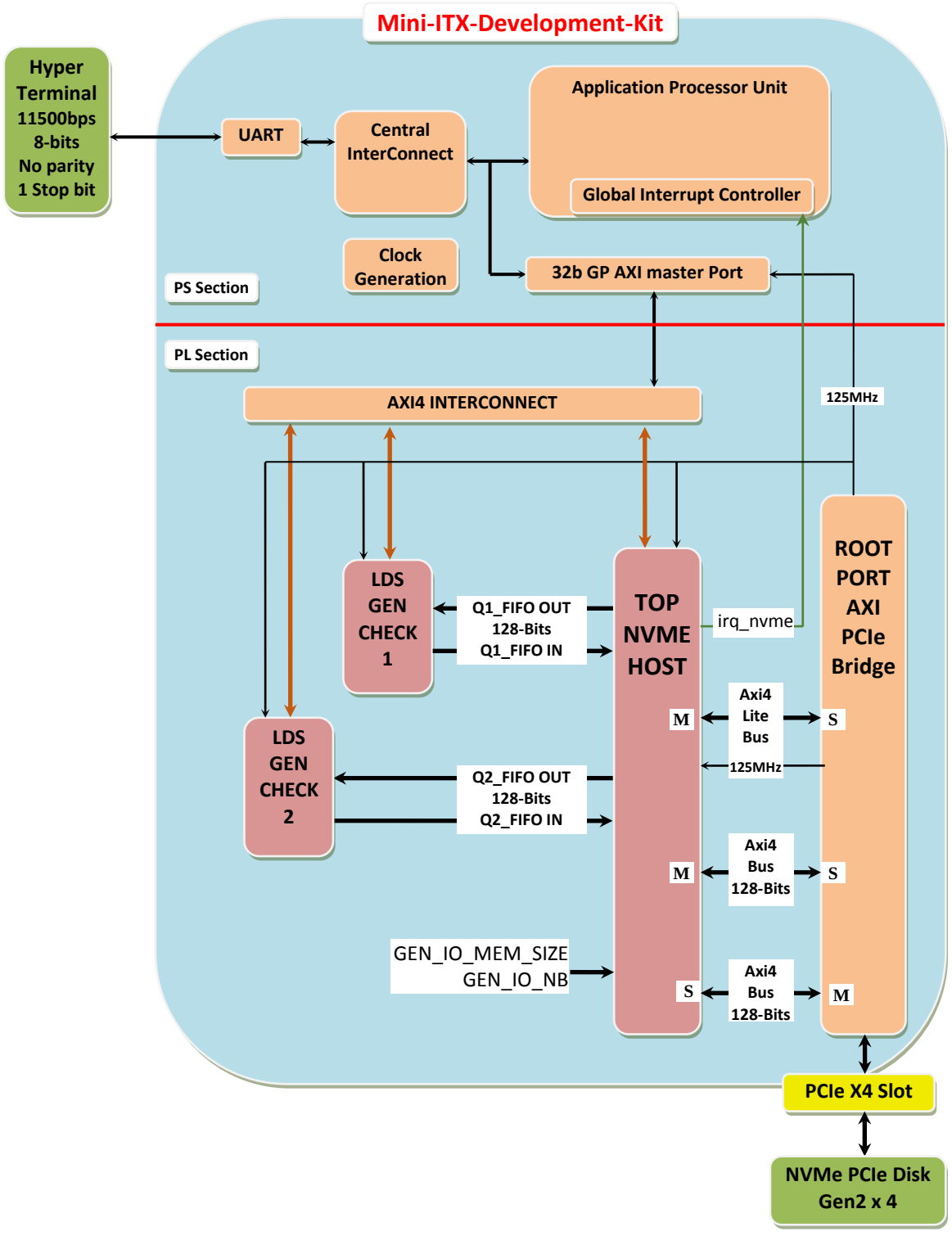
ITX Zynq 7
NVMe Host Recorder IP

CPU Demo provided under NDA



- The CPU demo runs at 125MHz and its goal is to check performance during long transfer.
- You can run a write and read performance test through a User Interface on the Hyper Terminal, please have a look on the demo documentation for details.
- The C source code is provided which enables the user to modify it to fit its project requirement.

Features

The LDS NVME HOST RECORDER IP has been done for beginners and expert in NVMe to drive NVMe PCIe SSD.

The register file interface simplify the management of the IP for CPU interface or State Machine interface using AXI bus:

- PCIe RP and EP register configuration is done automatically.
- NVMe register configuration is done automatically.
- Able to manage 8 Name Spaces.
- Able to manage until 16 IO Queue to fit specific user requirement.
    - Each IO Queue is independent.
- Able to manage 512Bytes or 4096Bytes sector size.
- Able to run nearly all Admin command in parallel of IO Queue.
- Many IO command already pre-defined to ease use of the IP.
- Configurable IO Queue buffer size to fit user memory requirement in case of small density FPGA: 32KB, 64KB, 128KB or 256KB.
- Able to read all PCIe RP and EP registers.
- Easy connection to embedded Root Port PCIe IP through AXI bus.

When using a PCIe RP IP configured in Gen2 the system frequency is at 150MHz.
When using a PCIe RP IP configured in Gen3 the system frequency is at 250MHz.

The source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Verification

The LDS NVME HOST RECORDER IP has been validated on the Avnet Mini-ITX Development Kit Board and several disks. List of disk available on request.

Performance

The demo provided makes a Disk Write and Read performance test on each disk connected.
A counter value is written on the disk and then read back and checked.
The performance depends on disk tested and memory configuration of the IP, especially for read performance.
As an example:

- PCIe Gen2 x 4 HHHL disk
- 100 Giga Byte data transfer.
- Sequential Write : 1.3 GBytes/s
- Sequential Read : 1.4 GBytes/s

Design Package

Device Family	**Xilinx Zynq 7 FPGA** **speed grade : 2**
Package file	**Source code or Source Encrypted or Synthesis Netlist.** Data Sheet, IP Interface Description and Constraint File.
Design Tool Used	Xilinx VIVADO 2018.2.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contract available.

Utilization

IP core only				
IP Configuration	**LUT**	**LUTRAM**	**FF**	**BRAM**
1 Queue – 32KBytes Buffer	11000	4000	7000	21
1 Queue – 64KBytes Buffer	11000	4000	7000	28
1 Queue – 128KBytes Buffer	11000	4000	7000	46
1 Queue – 256KBytes Buffer	11000	4000	7000	78
2 Queues – 32KBytes Buffer	13000	4400	8200	33
2 Queues – 64KBytes Buffer	13000	4400	8200	47
2 Queues – 128KBytes Buffer	13000	4400	8200	82
2 Queues – 256KBytes Buffer	13000	4400	8300	146

Until 16 Queues available.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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