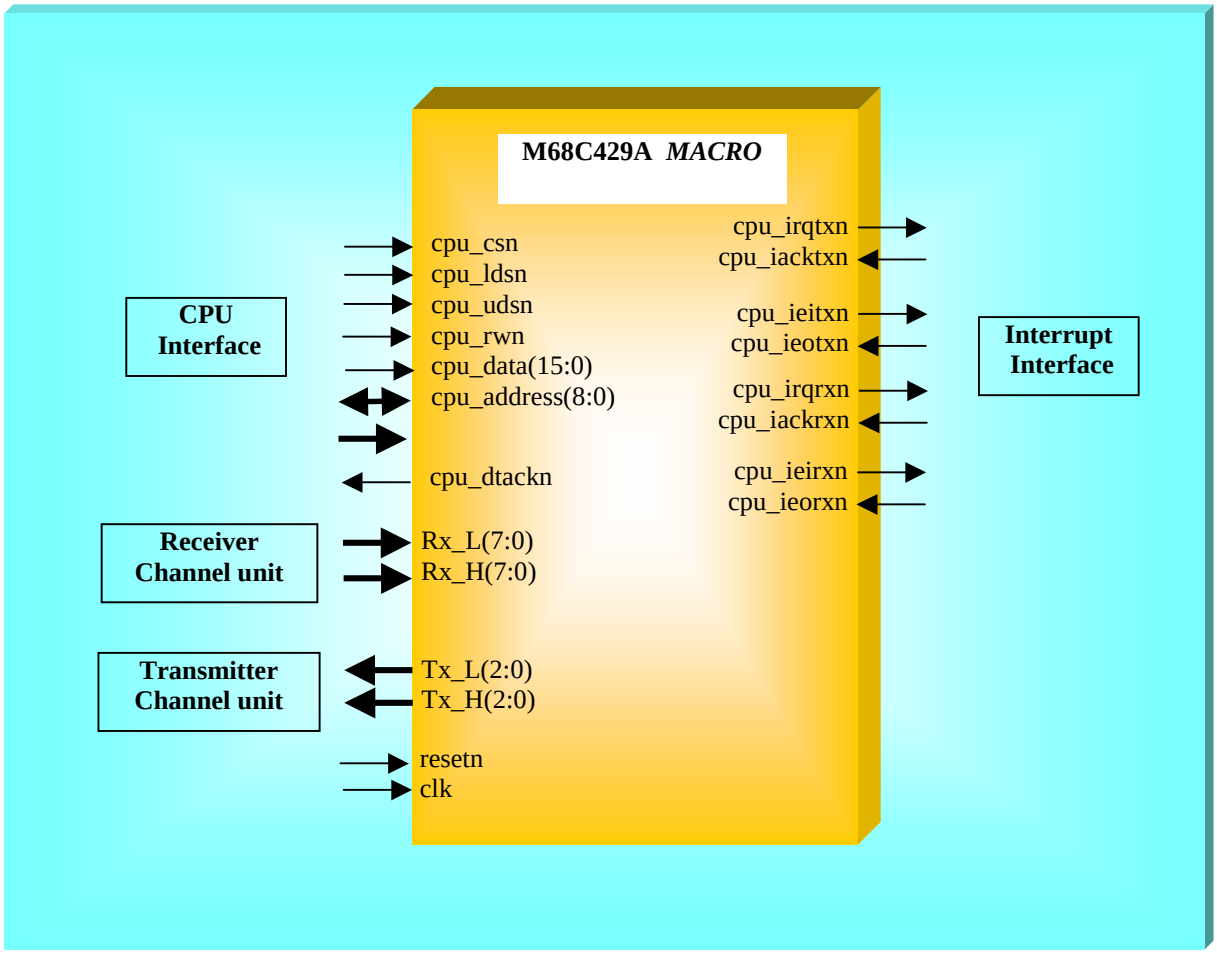
ARINC 429 Synchronous Multichannel Receiver / Transmitter VHDL *MACRO*

Product Brief

January 2004 – Ver. 1.3



Features

- 8 Independent Receivers (Rx)
- 3 Independent Transmitter (Tx) with FIFO
- 68000 microprocessor interface type
- 16-Bit Data-bus
- ARINC 429 Interface : '1' and '0' Lines, RZ code
- Support all ARINC 429 Data Rate Transfer and up to 2.5 Mbit/s
- Multi Label Capability
- Parity Control : Odd, Even, No Parity, Interrupt Capability
- Independent Interrupt Request Line for Rx and Tx Functions
- Vectored Interrupts
- Direct addressing of all Registers
- FPGA speed grade Operating Frequency dependant
- Available in VHDL source code format for ease of customization
- Can be customised by Logic Design Solutions

Design Package

Device Family	**PROASIC+ APA 300**	
core cells	**65% used ***	
Embedded Ram	**20 used (32 max)**	
I/O	**62 ****	
Package file options	**1**	**Bitstream + Data Sheet**
	2	**VHDL Source code** **VHDL Test Bench** for behavioural and gate level simulation. **Data Sheet** **User's guide :** Simulation, Synthesis and Place and Route procedures. **Constraint File**
Design Tool Used	VHDL synthesis Leonardo Spectrum or Synplify. VHDL ModelSim simulation tool from ModelTech. Actel Designer place and route software.	
Support	Support provided by Logic Design Solutions 6 months e-mail and telephone support from Logic Design Solutions included in the Macro price. Support does not cover User Macro modifications. Maintenance Contracts available.	

* Synthesis option dependant (area/speed)
**** Assuming all Macro signals are routed off chip.

General Description

The M68C429A is an ARINC 429 controller. It is based on TS68C429A but not strictly compatible with the TS68C429A. it is an enhanced version of the EF4442. The CPU interface is compatible with 16- or 32-bit microprocessor and the CPU interface can be customized on request.
.This macro can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with ARINC 429, VHDL, synthesis tools, Actel data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers macro integration and design services on FPGA.
Logic Design Solutions macros are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

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