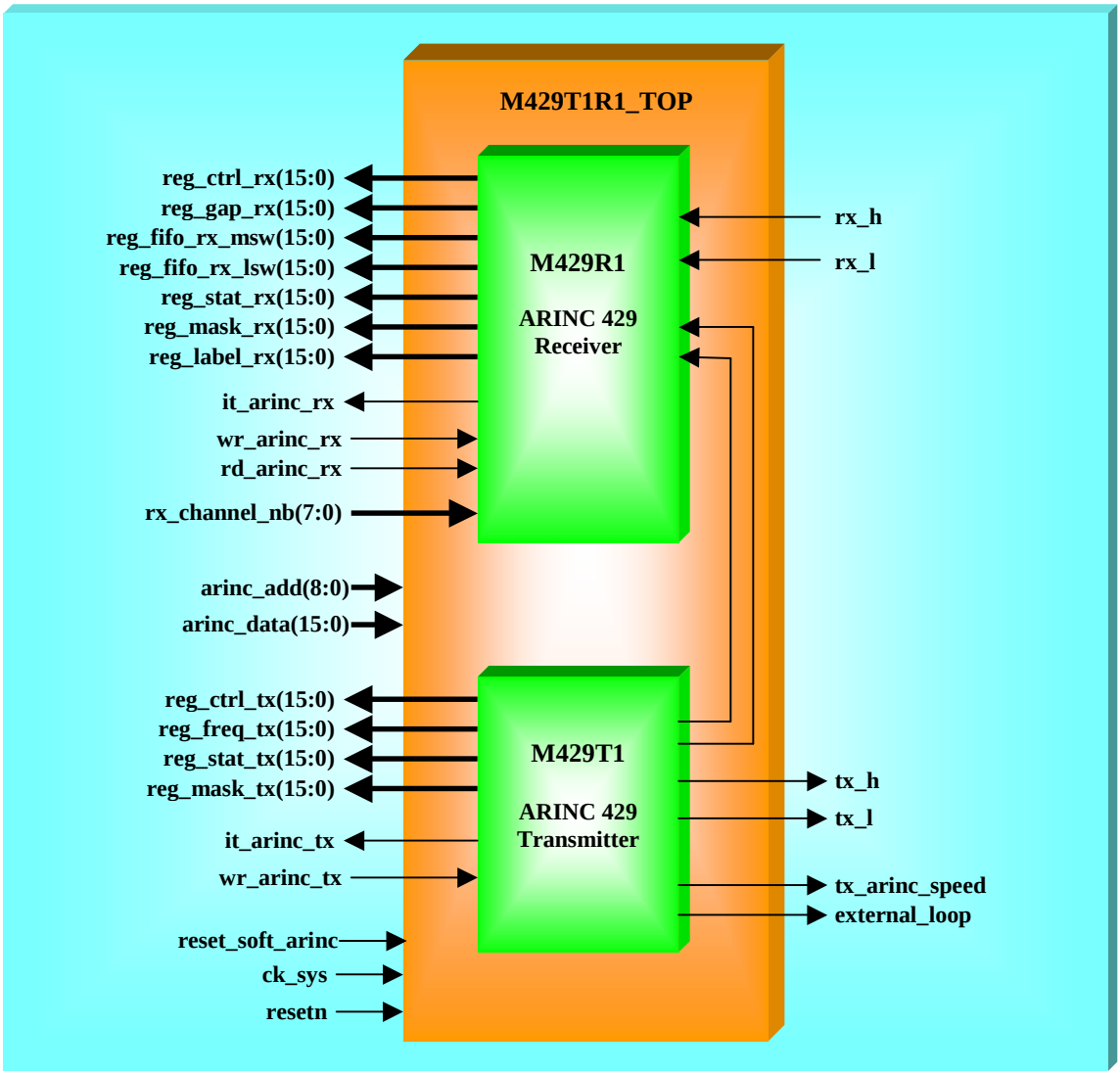
ARINC 429 Synchronous Receiver / Transmitter VHDL *MACRO*

Product Brief

February. 06 – Ver. 1.0



Features

- 1 Independent Receivers (Rx) with FIFO
- 1 Independent Transmitter (Tx) with FIFO
- Decoding signals interface type
- 16-Bit Data-bus
- Direct addressing of all Registers
- ARINC 429 Interface : '1' and '0' Lines, RZ code
- Support all ARINC 429 Data Rate Transfer and up to 2.5 Mbit/s
- Multi Label Capability
- Parity Control : Odd, Even, No Parity, Interrupt Capability
- Independent Interrupt Request Line for Rx and Tx Functions
- FPGA speed grade operating frequency dependant : system clock up to 70 MHz
- Available in VHDL source code format for ease of customization
- **DO254** design, verification and traceability documentation available on request
- Can be customized by Logic Design Solutions

Design Package

Device Family	Any FPGA		
Tiles	M429R1	631 – ProAsic + *	512 – ProAsic 3 *
	M429T1	600 – ProAsic + *	485 – ProAsic 3 *
	M429T1R1	1191 – ProAsic + *	980 – ProAsic 3 *
Block RAM	M429R1	3 – ProAsic +	2 – ProAsic 3 *
	M429T1	2 – ProAsic +	1 – ProAsic 3 *
	M429T1R1	5 – ProAsic +	3 – ProAsic 3 *
I/O	219 **		
Frequency	50Mhz – ProAsic +		70Mhz – ProAsic 3 *
Package file	**VHDL Source code** **VHDL Test Bench** for behavioural and gate level simulation. **Data Sheet** and **Reference Guide** **User's guide :** Simulation, Synthesis and Place and Route procedures. **Constraint File**		
Design Tool Used	VHDL synthesis Leonardo Spectrum. VHDL ModelSim simulation tool from ModelTech. Place and Route software according FPGA technology.		
Support	Support provided by Logic Design Solutions 6 months e-mail and telephone support from Logic Design Solutions included in the Macro price. Support does not cover User Macro modifications. Maintenance Contracts available.		

* Rounded Number.
****** Assuming all Macro signals are routed off chip.

General Description

The M429T1R1 macro implements a synchronous single-chip ARINC 429 Transmit and Receive Controller Macro capable of linking one CPU to one ARINC 429 bus. The macro controls all ARINC 429 bus specific sequences, protocol and timing. The M429T1R1 macro interface allows the parallel-bus microprocessor to communicate bidirectionally with the ARINC 429 bus. This macro can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with ARINC 429 standard, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers macro integration and design services on FPGA.
Logic Design Solutions macros are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

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