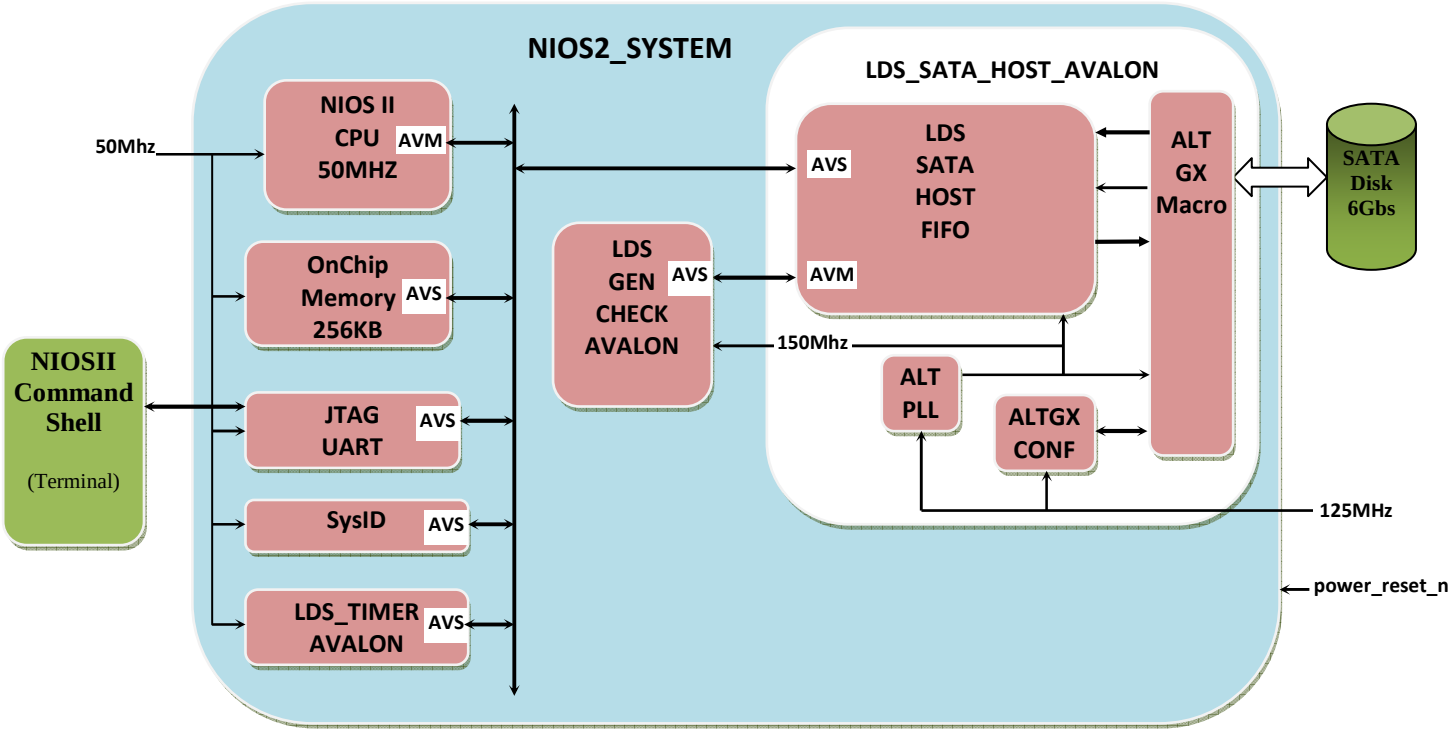
ARRIA V SATA 3 Host Controller
IP

Product Brief
May 14 – Ver. 1.0

QSYS Demo provided under NDA

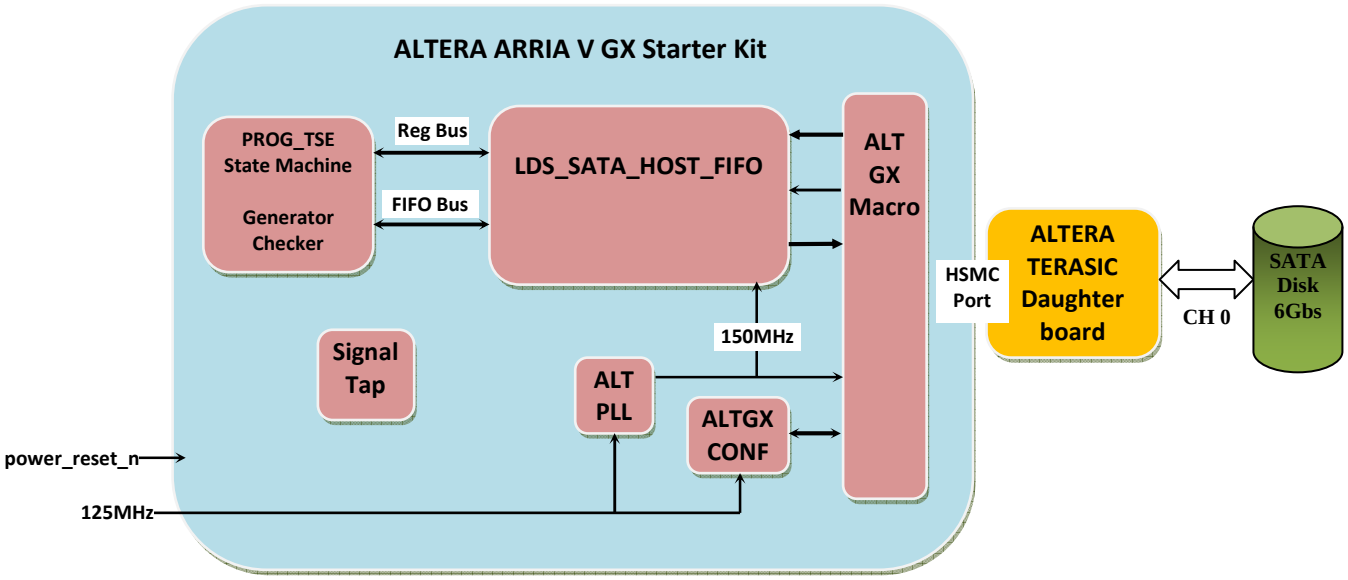


AVM : Avalon Master
AVS : Avalon Slave

- The Qsys demo runs at 150MHz and its goal is to check performance during long transfer.
- The C code provided is a sub-set of our SATA Recorder IP C code.
- You can run a write and read performance test through a User Interface on the Hyper Terminal, please have a look on the demo documentation.
- C code source is available with the demo, it can be modified to fit your project requirement.
- The Demo enables you to do only 32 Giga Bytes Write and Read Transfer, then you have to reset the board !

- Performance example :
  - Transfer Data : 80 Giga Byte data transfer with incompressible data.
  - SAMSUNG 840 PRO 256GB SSD
    - Sequential Write : 480 MBytes/s
    - Sequential Read : 500 MBytes/s
  - If NIOSII runs at a faster speed tan 50MHz the performance can be increased.

State Machine Demo provided under NDA



This design helps you to understand how you can manage the LDS SATA IP from a State Machine.

1) At reset the test is run.
2) The result of the test and several signals can be observed from Signal Tap.

Features

Rate Match FIFO

- Manage SATA reference frequency difference between the FPGA and the Disk

Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provide a 32 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding
- Fixed Speed 6Gbs or 3Gbs

Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Enable BIST Retimed loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- The interface between the link layer and the transport layer is 32-bit wide

Transport Layer features

- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability

- DMA interface can be connected easily to memory space or FIFOs
- Support DMA Abort primitive
- 128-Word Ingress and Egress FIFO between Transport and Link Layer
- NCQ Support

General Description

The LDS_SATA3_HOST_AR5GX IP incorporates the Transport layer, the Link layer, the PHY layer and the Rate Macth FIFO on a ALTERA Stratix IV GX FPGA. The LDS_SATA3_HOST_AR5GX IP is compliant with Serial ATA III specification and signaling rate is 6Gbps and scalable 3Gbs. The LDS_SATA3_HOST_AR5GX X IP is fully synchronous with system frequency (Clock_sys) at 150MHz in case of 6Gbps speed selection and 75MHz in case of 3Gbs speed configuration. The VHDL source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.

Verification

The LDS_SATA_HOST_AR5GX IP has been validated on the ALTERA ARRIA V GX Starter Kit and several disks.

Design Package

Device Family	**ALTERA ARRIA V GX FPGA – speed grade : Lowest**
ALM used	3200
M10K Blocks	19
Package file	**Synthesis Netlist :** Data Sheet, Quartus project Description and Constraint File
	VHDL Source code : Data Sheet , Quartus project Description and Constraint File.
Design Tool Used	ALTERA QUARTUS II v13.1 VHDL ModelSim simulation tool from ModelTech.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

General Description

The LDS_SATA_HOST_AR5GX IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA_HOST_R5GX IP is available only on ALTERA ARRIA V GX FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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