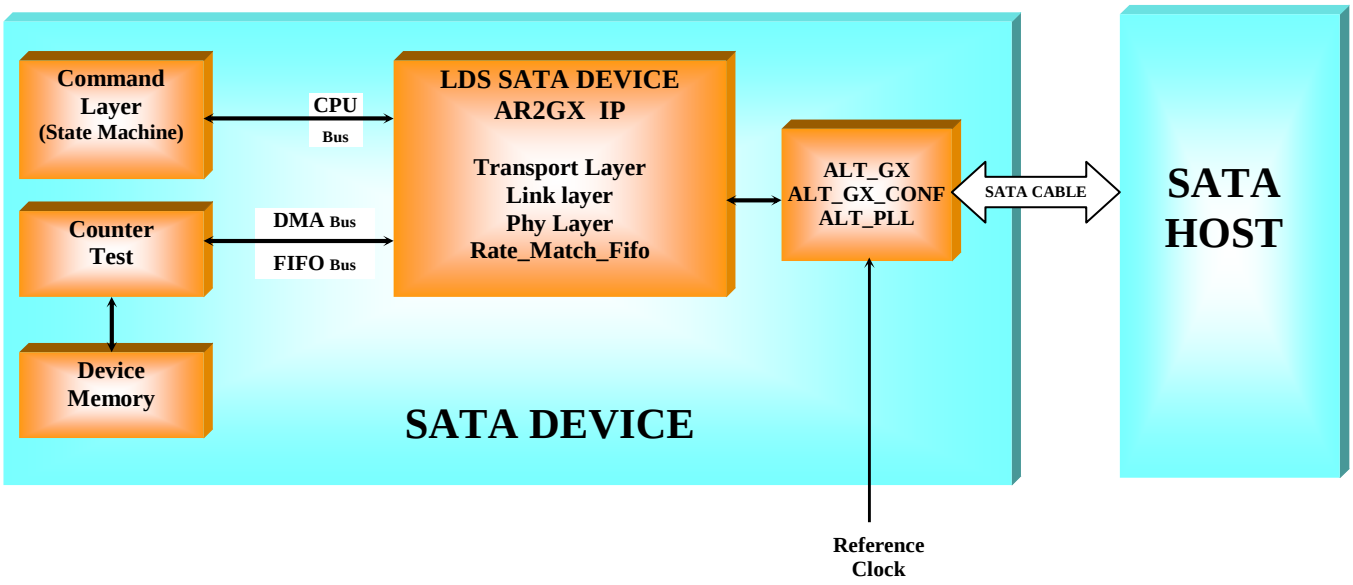
Serial ATA DEVICE Controller AR2GX
VHDL *IP*

Product Brief

April 12 – Ver. 1.0



Features

The LDS_SATA_DEVICE_AR2GX IP incorporates the Transport layer, the Link layer, the PHY layer and the Rate Macth FIFO on a ALTERA ARRIA II GX FPGA. The LDS_SATA_DEVICE_AR2GX IP is compliant with Serial ATA II specification and signaling rate is 1.5Gbps and scalable 3Gbs. The LDS_SATA_DEVICE_AR2GX IP is fully synchronous with system frequency (Clock_sys) at 37.5MHz in case of 1.5Gbps speed selection and 75MHz in case of 3Gbs speed selection. The VHDL source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.

Rate Match FIFO

- Manage SATA reference frequency difference between the HOST and the Device

Physical Layer features

- Detect and generate OOB sequence
- Detect the K28.5 comma character and provides a 16 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in ALTERA ALT_GX Macro
- Manages 1.5Gbs or 3Gbs data rate

Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 generation and check
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- The interface between the link layer and the transport layer is 32-bit wide

Transport Layer features

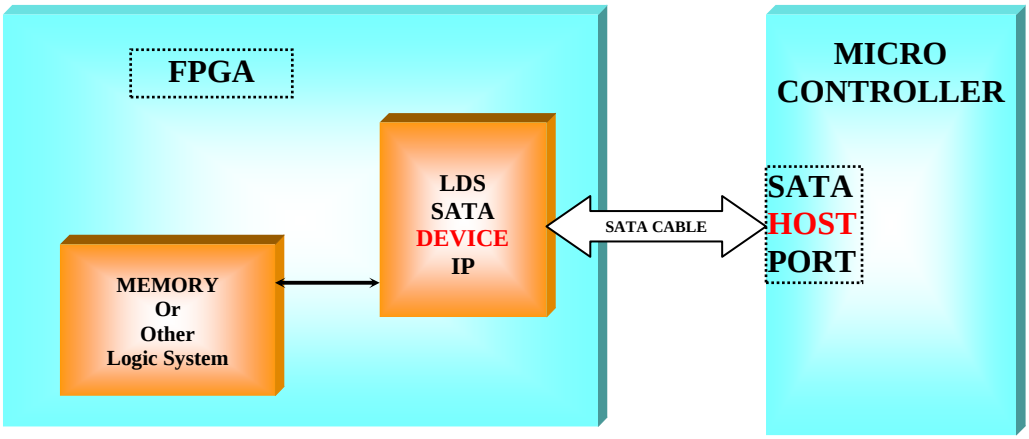
- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs
- Support DMA Abort primitive

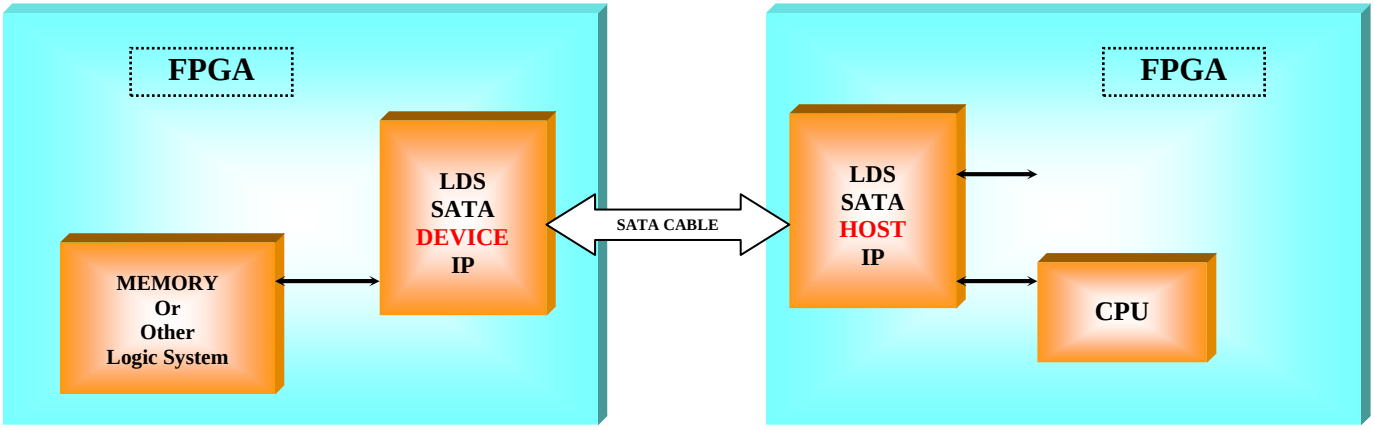
Command Layer features

- The Command Layer is always provided in Source code.
- The customer is able to modify the command layer.
- The Command layer is managing by default :
  - IDENTIFY DEVICE
  - IDLE (NON DATA Protocol)
  - READ_SECTOR_EXT (PIO-IN Protocol)
  - WRITE_SECTOR_EXT (PIO-OUT Protocol)
  - READ_DMA_EXT (DMA IN Protocol)
  - WRITE_DMA_EXT (DMA OUT Protocol)
  - SOFTWARE RESET Protocol
  - HARDWARE RESET Protocol

Application Example

The SATA Standard can be used to transfer data between a Microcontroller and a FPGA, or from a FPGA to another FPGA.





Verification

The LDS_SATA_DEVICE_AR2GX IP has been validated on the ALTERA ARRIA II GX development board.

Performance

The LDS_SATA_HOST IP has been connected to the LDS_SATA_DEVICE IP.
A 500Gbytes transfer is done at 270MB/s in sequential write and 280MB/s in sequential read – DMA transfer of 2048 sectors.

Design Package

Device Family	**ALTERA ARRIA II GX FPGA – speed grade : Lowest**
ALUT used	3000
Total register	3000
Package file	**Synthesis Netlist :** Data Sheet, Quartus project Description and Constraint File
	VHDL Source code : Data Sheet , Quartus project Description and Constraint File.
Design Tool Used	ALTERA QUARTUS II v11.0 VHDL ModelSim simulation tool from ModelTech.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

General Description

The LDS_SATA_DEVICE_AR2GX IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA_DEVICE_AR2GX IP is available only on ALTERA ARRIA II GX FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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