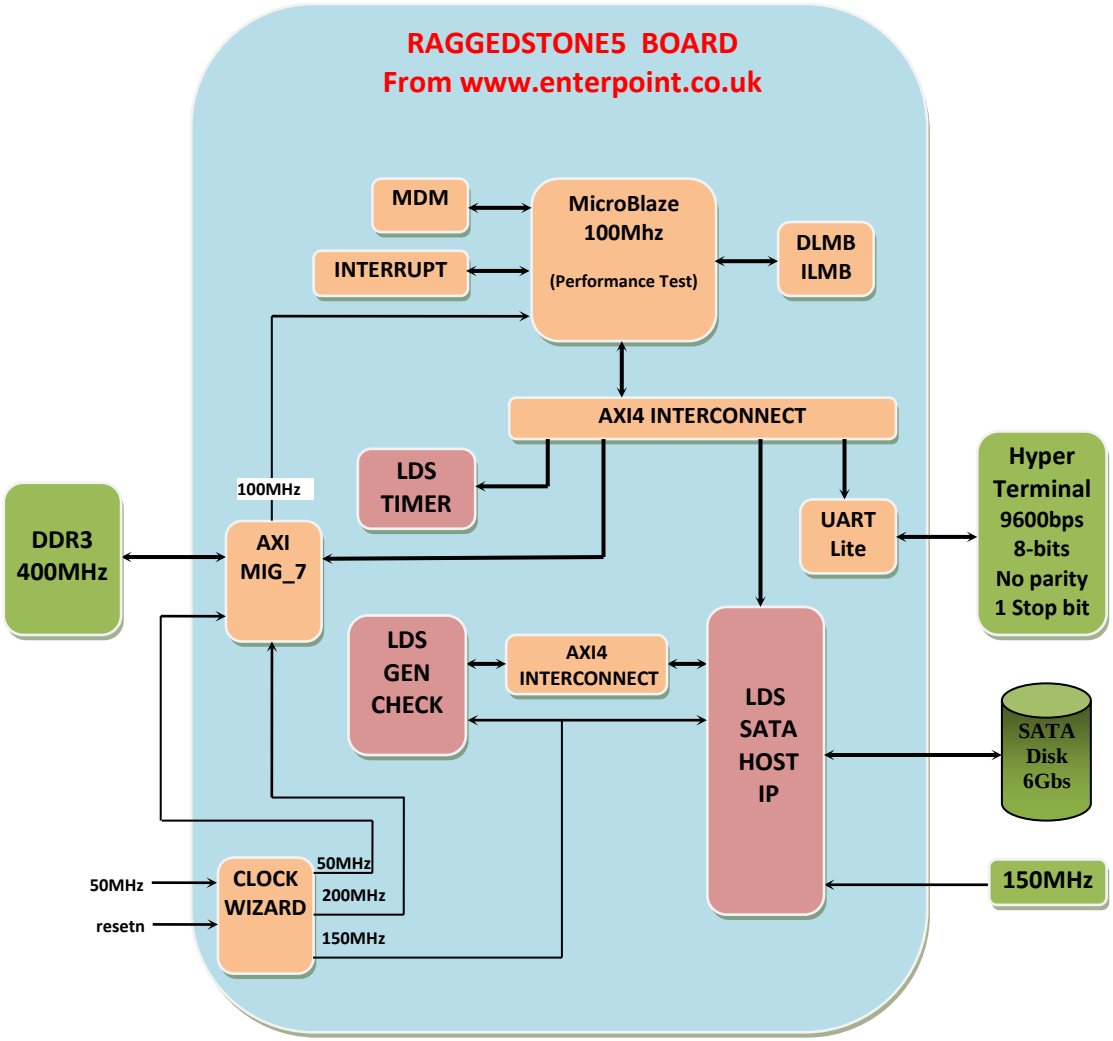
Artix 7 SATA 3 Host Controller
IP

Product Brief

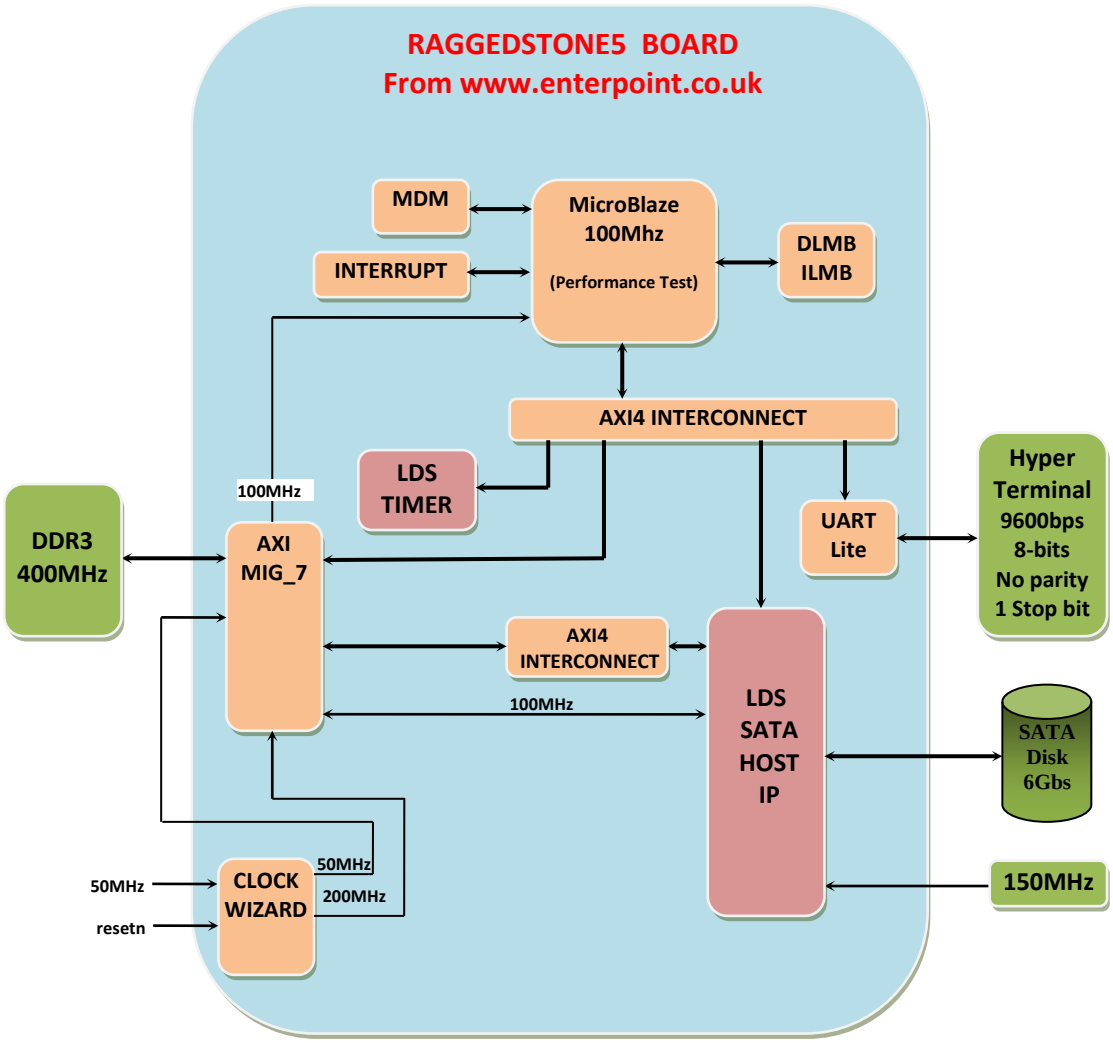
Jun. 16 – Ver. 1.0

MicroBlaze Demo 1 provided under NDA



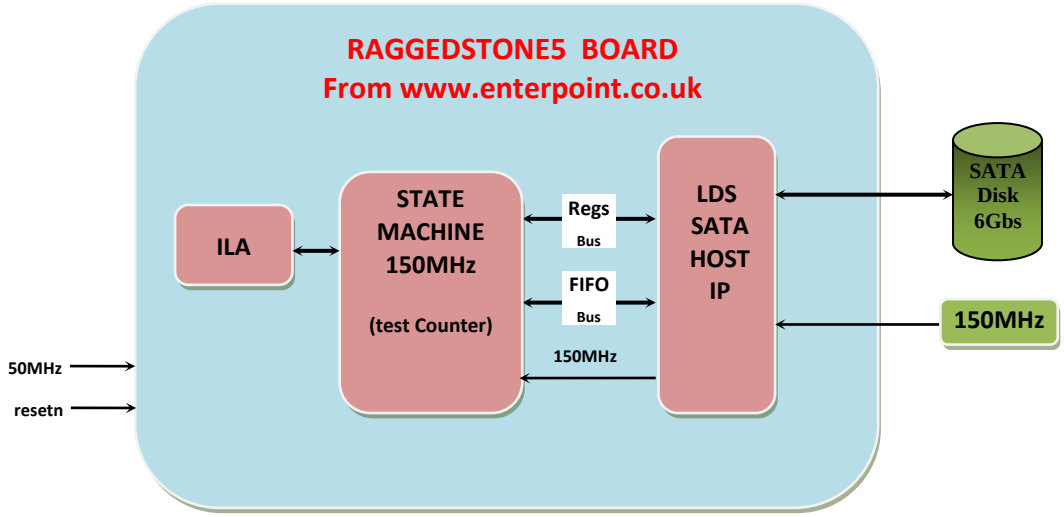
- The demo 1 runs at 150MHz and its goal is to check performance during long transfer. The transfer size is not limited by the size of the DDR as in demo 2.
- The C source code provided is a sub-set of our SATA Recorder IP C source code.
- You can run a write and read performance test though a User Interface on the Hyper Terminal, please have a look on the demo documentation.
- C source code is available with the demo, it can be modified to fit your project requirement.
- The Demo enables you to do only 32 Giga Bytes Write and Read Transfer, then you have to reset the board !

MicroBlaze Demo 2 provided under NDA



- The C source code provided is a sub-set of our SATA Recorder IP C source code.
- You can run a write and read performance test through a User Interface on the Hyper Terminal, please have a look on the demo documentation.
- C source code is available with the demo, it can be modified to fit your project requirement.
- Transfer size is limited by the DDR3 memory size.
- The Demo enables you to do only 32 Giga Bytes Write and Read Transfer, then you have to reset the board !

State Machine Demo 3 provided under NDA



This design helps you to understand how you can manage the LDS SATA IP from a State Machine.

1) At reset the test is run
2) The result of the test and several signals can be observed from Chipscope pro

Features

The LDS_SATA3_HOST_XA7 IP incorporates the Transport layer, the Link layer and the PHY layer on a Xilinx Artix 7 speed grade 2 FPGA. The LDS_SATA3_HOST_XA7 IP is compliant with Serial ATA III specification and signaling rate is fixed to 6Gbs. The LDS_SATA3_HOST_XA7 IP is fully synchronous with system frequency (Clock_sys) at 75MHz in case of 3Gbs speed selection and 150MHz in case of 6Gbs speed selection. The source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.

Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provides a 32 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in FPGA Serdes
- 6Gbs or 3Gbs Speed

Link Layer features

- Scrambling of TX data and descrambling of RX data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- CONT primitive management in receive and transmit
- The interface between the link layer and the transport layer is 32-bit wide

Transport Layer features

- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs (FIFO interface provided)
- NCQ Support.

Verification

The LDS_SATA3_HOST_XA7 IP has been validated on the Raggestone5 Board from Enterpoint and several disks.
List of disk available on request.

Performance

The demo provided makes a Disk Read and Write performance test on each disk connected. A counter value is written on the disk and then read back.

- Transfer Data: 80 Giga Byte data transfer with incompressible data.
- SAMSUNG 840 PRO 256GB SSD
  - Gen 3 Sequential Write : 500 MBytes/s
  - Gen 3 Sequential Read : 530 MBytes/s
  - Gen 2 Sequential Write : 254 MBytes/s
  - Gen 2 Sequential Read : 270 MBytes/s

Design Package

Device Family	**Xilinx Artix 7 FPGA** **Gen 3 : speed grade 3/2 *** **Gen 2 : speed grade 2**
Number of occupied Slices	1000 (IP core only)
Package file	**Source code or Synthesis Netlist :** Data Sheet, AXI SATA HOST Interface Description and Constraint File.
Design Tool Used	Xilinx VIVADO 2016.1
Support	Support provided by Logic Design Solutions 1 year e-mail and phone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

* For Gen3, speed grade 3 can be required, it will depend on your design and place & route result. At Gen3 the IP runs at 150 Mhz which can be a frequency too high for a speed grade 2. Floor planning of the IP can be necessary to reach the frequency.

General Description

The LDS_SATA3_HOST_XA7 IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA3_HOST_XA7 IP is available only on Xilinx Artix 7 FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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