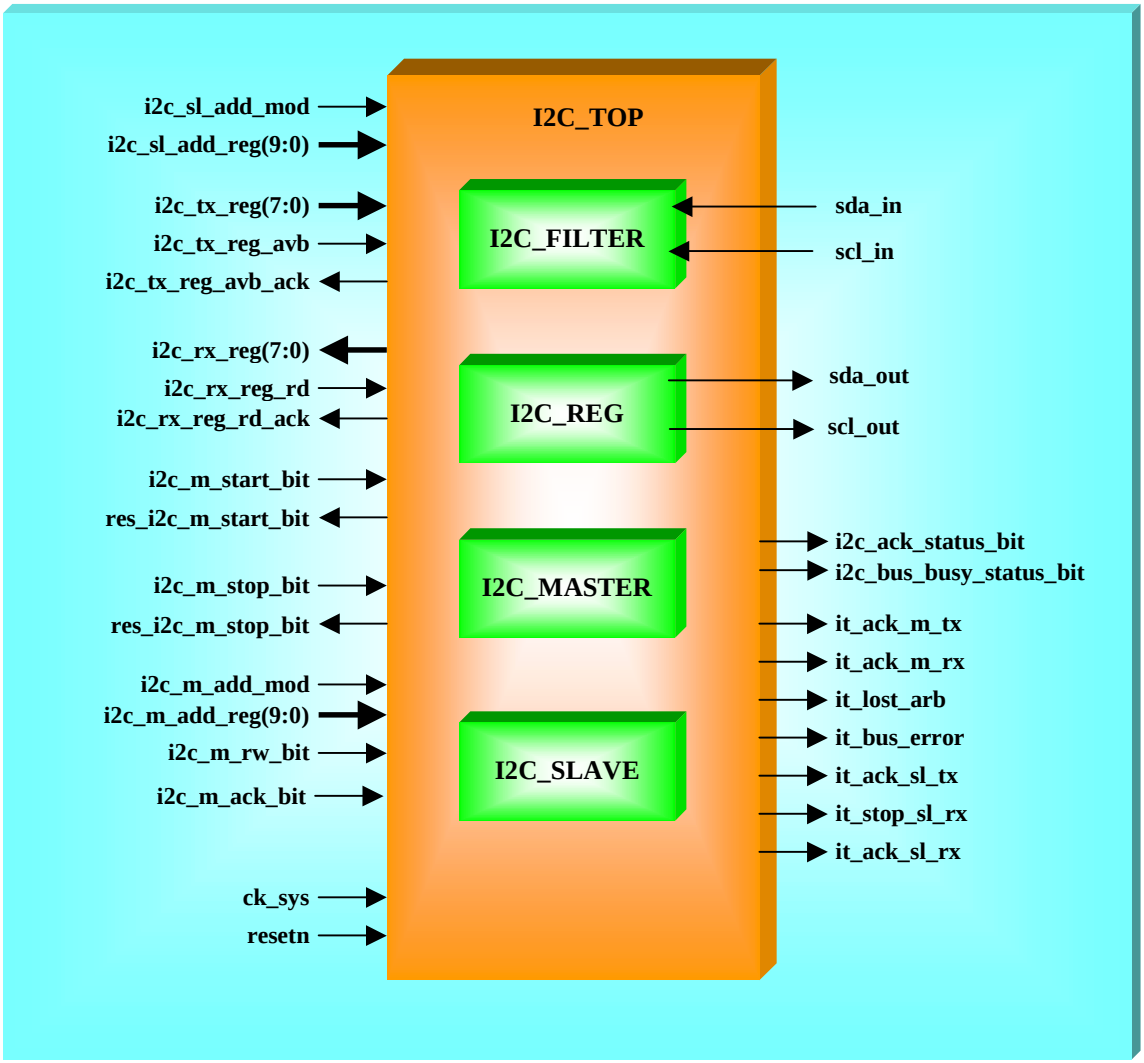
I2C Master Slave
VHDL *MACRO*



Features

- Single-chip synchronous I2C Master and Slave Macro in FPGA (I2C is a trademark of Philips, Inc)
- Designed to be included in high-speed and high-performance applications
- Direct Connection to CPU register set
- Compliant with I2C-bus specification version 1.0
- Standard mode operation (100Kbits)
- Multi-master operation with arbitration and clock synchronisation (only master)
- Support for reads and writes only
- 7-bit and 10-bits address management
- Synchronised on system clock
- Hardware digital filter on SCL and SDA signals
- No support of general call
- FPGA speed grade operating frequency dependant : system clock up to 180 MHz
- Available in VHDL source code format for ease of customization
- Can be customised by Logic Design Solutions

Design Package

Device Family	**Any FPGA**
LUT	**320** *
Tiles	**765 ***
I/O	**61** **
Package file	**VHDL Source code** **VHDL Test Bench** for behavioural and gate level simulation. **Data Sheet** and **Reference Guide** **User's guide :** Simulation, Synthesis and Place and Route procedures. **Constraint File**
Design Tool Used	VHDL synthesis Leonardo Spectrum. VHDL ModelSim simulation tool from ModelTech. Place and Route software according FPGA technology.
Support	Support provided by Logic Design Solutions 6 months e-mail and telephone support from Logic Design Solutions included in the Macro price. Support does not cover User Macro modifications. Maintenance Contracts available.

* Rounded Number.
****** Assuming all Macro signals are routed off chip.

General Description

The MI2CMS macro implements a synchronous single-chip I2C Master and Slave Macro capable of linking one CPU to one I2C-bus. Communication with I2C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all I2C-bus specific sequences, protocol, arbitration and timing. The I2C macro interface allows the parallel-bus microprocessor to communicate bidirectionnally with the I2C-bus.This macro can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with I2C V(1.0) standard, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers macro integration and design services on FPGA.
Logic Design Solutions macros are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

Logic Design Solutions
106 Boulevard de la Résistance
93460 Gournay sur Marne – France.
Phone : +33 (0) 1 45 92 24 47
Fax : +33 (0) 1 45 92 22 10
E-mail : info@logic-design-solutions.com
WEB: http://www.logic-design-solutions.com