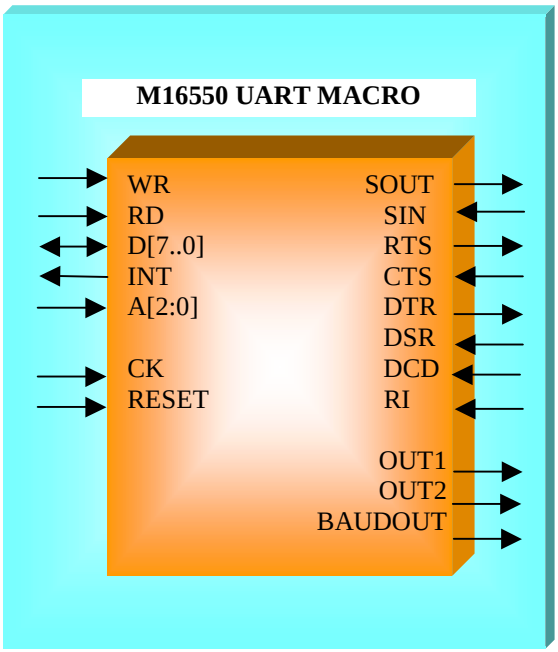
Universal Asynchronous Receiver / Transmitter with FIFO *MACRO*

Product Brief
Aug. 99 – Ver. 2



Features

- Single-chip synchronous UART
- Functionally based on the National Semiconductor Corporation NS16550 device
- Designed to be included in high-speed and high-performance applications
- System clock up to 150 MHz
- CPU independent interface
- Complete asynchronous communication protocol including :
  - 5,6,7 or 8-bit data transmission
  - Even/Odd or no parity bit generation and detection
  - Start and Stop bit generation and detection
  - Line break generation and detection
  - Receiver Overrun and framing detection
  - Up to 1M baud (system frequency dependent)
- 1 to 65535 divisor generates 16X clock
- Buffered transmit and receive registers
- Transmitter and receiver are buffered with 16 Byte FIFO, plus 3 error bits per data byte on receiver
- Polled or interrupt mode
- Loopback mode

Design Package

Device Family	**Any FPGA**
LUTs	120 *
I/O	27 **
System Clock	Up to 150 MHz
Documentation	**VHDL Source code** **VHDL Test Bench** for behavioural and gate level simulation. **Data Sheet** and **Reference Guide** **User's guide :** Simulation, Synthesis and Place and Route procedures. **Constraint File**
Design Tool Requirement	VHDL synthesis Leonardo Spectrum. VHDL ModelSim simulation tool from ModelTech. Place and Route software according FPGA technology..
Support	Support provided by Logic Design Solutions 6 months e-mail and telephone support from Logic Design Solutions included in the Macro price. Support does not cover User Macro modifications. Maintenance Contracts available.

***** Rounded Number.
****** Assuming all Macro signals are routed off-chip.

General Description

The macro M16550, implements a synchronous universal asynchronous receiver/transmitter, which provides an interface between a microprocessor and a serial communication channel.
This macro can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with VHDL, synthesis tools, FPGA data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers macro integration and design services on FPGA.
Logic Design Solutions macros are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

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