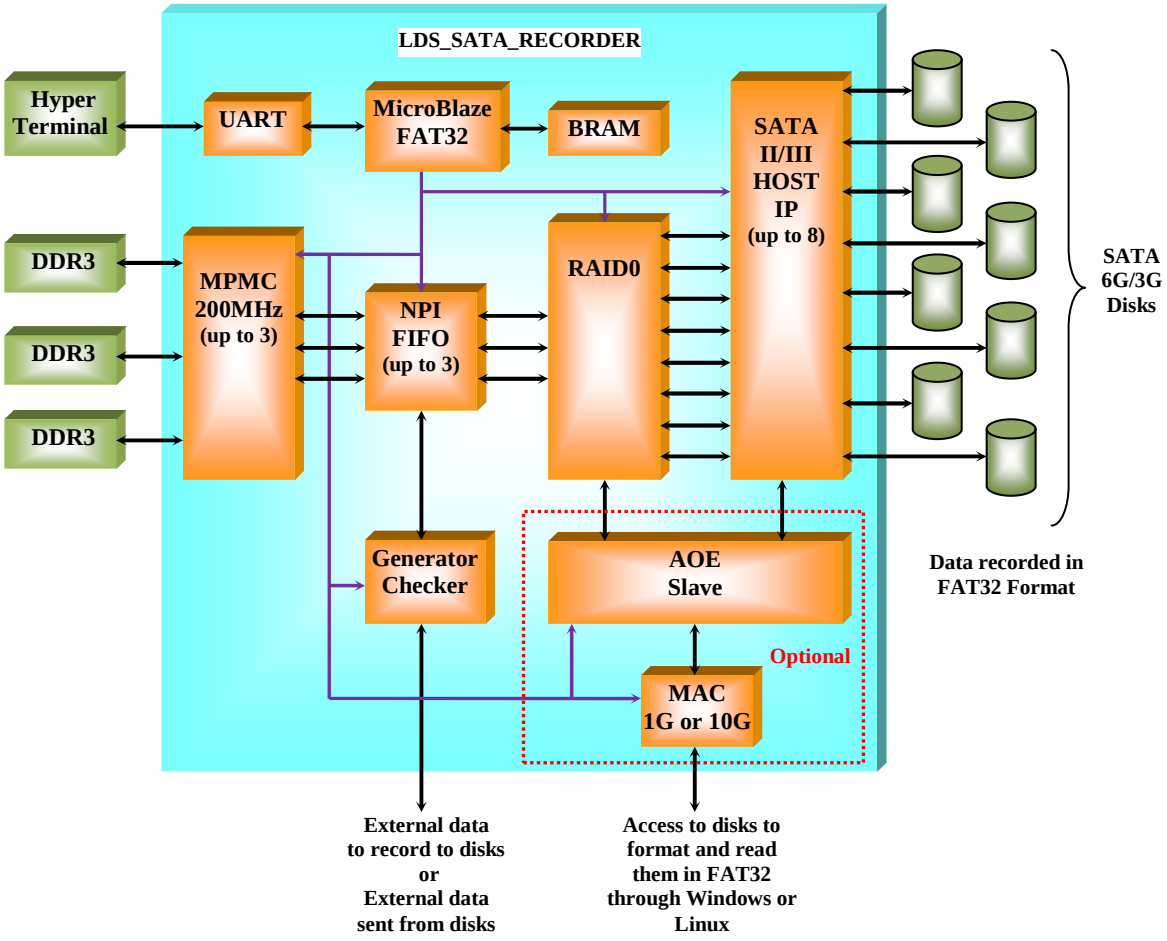
Fast, Compact and Configurable
SATA Recorder XV6 *IP*

Product Brief

May 12 – Ver. 1.0



Features

The LDS_SATA_RECORDER_XV6 IP is a complete recorder system IP. It can be configured according the recording performance required and the quantity of the data to record.

- The data can be recorded in FAT32 or in RAW format. In FAT32 mode, the disks must be already formatted or can be formatted through the Ethernet link and a PC under windows or Linux (free driver).
- The Ethernet link, when used, enables to download FAT32 files into your PC to process them later according user application.
- The 'Generator_Checker' block enables to check any recording error in the data flow.This block generates a counter which is written into disks and then readback and compared in order to detect any recording error. External data goes through this block.
- A User Interface on a Hyperterminal enables to configure all the recording session (recording size, file size, raid0 strip, number of disk, read directory, etc…) and enables to run a write and read performance test of the system using the 'Generator_Checker' block. It enables you to chek the performance of your systems, especially the disks.

Netlist and VHDL source code format is available for ease of customization. The C source code is always provided. The customization can be done by Logic Design Solutions.

SATA Features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provide a 16 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in Xilinx SERDES
- Auto Speed negotiation (Gen 2 or Gen 3)
- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- The interface between the link layer and the transport layer is 32-bit wide
- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- NCQ supported (not used in Recorder application)

AoE Features

- Manages AoE protocol
- Manages jumbo frame until 9216 bytes
- Do not support Cache write data
- Manages all Config/Query messages
- 1Gbits Mac using embedded MAC in GMII or RGMII.
- 10Gbits Ethernet Mac with XGMII or XAUI interface.

Verification

The LDS_SATA_RECORDER_XV6 IP has been validated on a

- Xilinx ML605 + XM104 Board.

- Custom BOARD : **MSE-RECORDER-XV6.** This board has been designed for ONERA 'THE FRENCH AEROSPACE LAB' by ESTAR Company.

ONERA
THE FRENCH AEROSPACE LAB

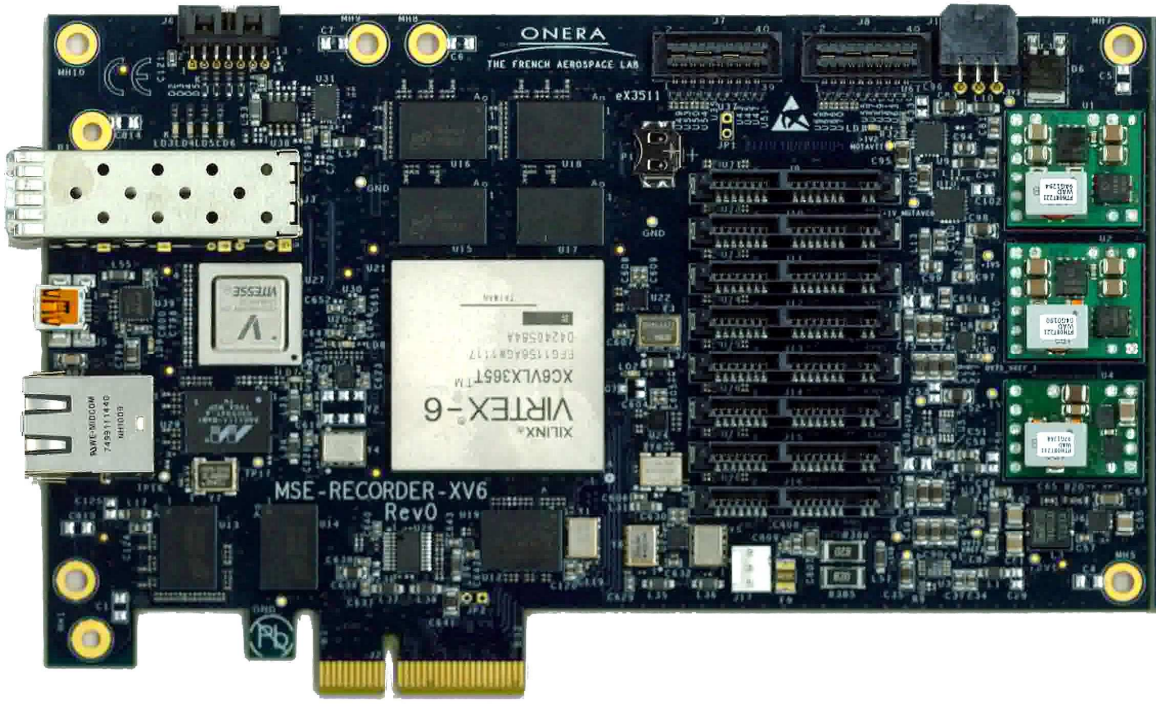
ESTAR

You can buy the **MSE-RECORDER-XV6** Board through Logic Design Solutions.

We can define a complete system for you including disks.

MSE-RECORDER-XV6 Board Features :

- FPGA Xilinx Virtex-6 LX365T -2 or -3
- 8 x SATA III (6Gb/s)
- Ethernet 10G SFP+ and 1G
- 1.5GB DDR3 - 533MHz
- 2 x SAMTEC QSH (43.2Gb/s perc connector)



Performance

The demo provided on the Custom BOARD makes a Disk Read and Write performance test on 8 disks in RAID0. A counter value is written on the disk and then read back.
Example : Intel SSD 510 Series 6Gbs => 800Gbytes transfer at 1.5GB/s sustain transfer in sequential write and 360MB/s in sequential read – DMA transfer of 256 sectors.

The demo provided on the Xilinx ML605 Evaluation board + XM104 daughter board makes makes a Disk Read and Write performance test on 2 disks in RAID0. A counter value is written on the disk and then read back.
Example : Intel SSD 510 Series 3Gbs => 200Gbytes transfer at 400MB/s sustain transfer in sequential write and 360MB/s in sequential read – DMA transfer of 256 sectors.

A bitsream demo is available on a Xilinx ML605 + XM104 board in SATA II configuration and 1G Ethernet.

Design Package

Device Family	**Xilinx Virtex 6 LXT/SXT FPGA** **speed grade : 1 => SATA 3Gbs** **speed grade : 2 => SATA 6Gbs** **speed grade : 3 => Best throuput** (under test)
Number of occupied Slices	Depend on recording system configuration. With biggest configuration LXT365 is recommended.
Package file	**Netlist or VHDL Source code :** Data Sheet , EDK project Description, C source code and Constraint File.
Design Tool Used	Xilinx XST VHDL synthesis. VHDL ModelSim simulation tool from ModelTech. Xilinx ISE Place and Route software.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

General Description

The LDS_SATA_RECORDER_XV6 IP is a complete recorder system IP. It can be configured according the recording performance required and the quantity of the data to record. The LDS_SATA_RECORDER_XV6 IP is available only on Xilinx Virtex 6 LXT/SXT FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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