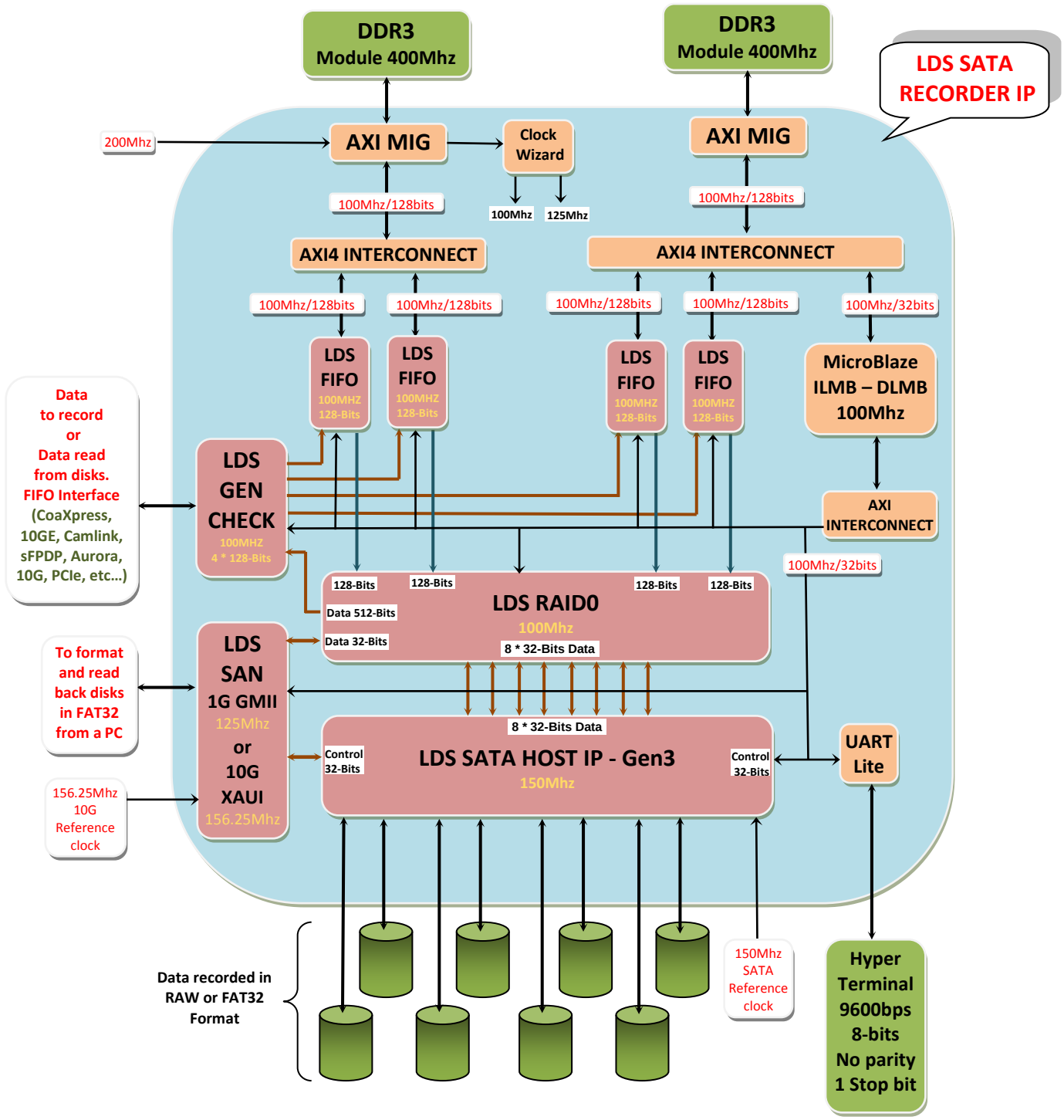
Fast, Compact and Configurable
SATA Recorder XA7 *IP*

Product Brief

Oct. 16 – Ver. 1.0



Features

The LDS_SATA_RECORDER_XA7 IP is a complete recorder sub-system IP. It can be configured according to the recording performance required and the quantity of the data to be recorded.

- The data can be recorded in FAT32 or in RAW format.

- The Ethernet link, when used, enables to download FAT32 files into your PC to process them later according to user application (It is not intended to record data, but it can do).
  - 1Gbits LDS Mac in GMII or 10Gbits Ethernet LDS Mac with XGMII or XAUI interface.
  - Manages jumbo frame until 9216 bytes
  - Manages AoE protocol in State Machine

- The 'Generator_Checker' block enables to check any recording error in the data flow. This block generates a counter which is written into disks and then readback and compared in order to detect any recording error. The user data goes through this block with the help of asynchronous internal FIFO.

- A User Interface on a Hyperterminal enables to configure all the recording session (recording size, file size, raid0 strip, number of disk, Directory, etc…) and enables to run a write and read performance test of the system using the 'Generator_Checker' block. It enables you to check the performance of your systems, especially the disks.

Netlist and VHDL source code format is available for ease of customization. The C source code is always provided. It can be customized by Logic Design Solutions.

Verification

The LDS_SATA_RECORDER_XA7 IP has been validated on a RAGGEDSTONE5 evaluation board from Enterpoint and SSD.

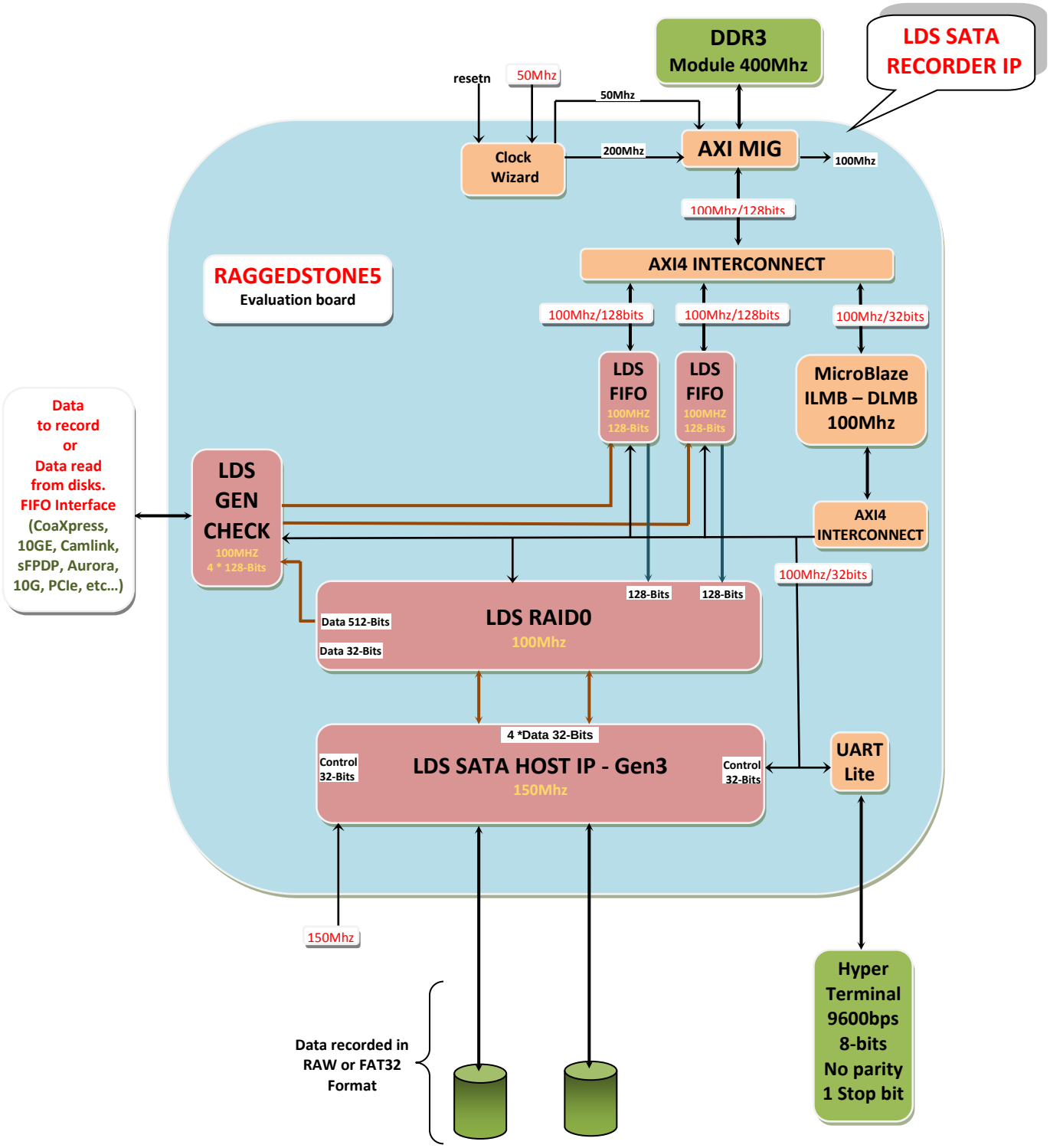
Design Package

Device Family	**Xilinx ARTIX 7 T FPGA** **speed grade : 2**
Package file	**Netlist or VHDL Source code:** Data Sheet, Project Description, C source code and Constraint File.
Design Tool Used	Xilinx VIVADO 2015.2
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

Demo Package

One bit stream demo is available on a RAGGEDSTONE5 board in SATA III or SATA II configuration.

The demo configuration is the following:



Performance

The demo provided on the RAGGEDSTONE5 board undertakes a Disk Read and Write performance test on 2 disks in RAID0. A counter value is written on disks and then read back.

Recording performance :

- Two SAMSUNG 840 PRO 6Gbs :
  - 80 GBytes transfer at 770MB/s sustain transfer in sequential write
    - The performance is limited by the DDR3 FIFO. The usual performance is 980MB/s.
  - 80 GBytes transfer at 1050MB/s sustain transfer in sequential read
  - Recorder configured with 8192 sectors per ATA command.

Ethernet performance :

- **1G SAN**:
  - Read 100Mbyte/s
  - Write 100Mbyte/s

- **10G SAN**:
  - One disk Read : 350Mbyte/s
  - Three disks Read in same time : 850Mbyte/s
  - One disk Write : 310Mbyte/s
  - Three disks Write in same time : 750Mbyte/s

Available Configuration

The Recorder IP is configurable according to user needs, the possible options are:

- **FAT32 :** if the user needs to read back recorded data on a PC or through Ethernet. Disks must be formatted before used with the recorder IP. If FAT32 is not needed, the data are recorded in RAW format by default.

- **1G SAN:** if the user needs to read back recorded data through Ethernet.100MBytes/s Ethernet bandwidth. Either 1G_SAN or 10G_SAN are selectable not both.

- **10G SAN:** if the user needs to read back recorded data through Ethernet. Until 850MBytes/s Ethernet read bandwidth. Either 1G_SAN or 10G_SAN are selectable not both.

- **MIG – LDS_FIFO:** if the user does not have a data buffer in its data path.
  - One MIG is usually coupled with 2 LDS_FIFO which enables to have a 256-bits data path at 100 MHz.
  - In case of two MIGs, each MIG is connected to two LDS_FIFO which enabled to have a 512-bits data path at 100 MHz.

- **RAID0:** if the user needs to increase recording performance. It manages up to eight SATA IP.

- **SATA HOST:** One to eight SATA HOST IP to drive disks.

- **MicroBlaze:** It manages the data flow and the User Interface through the UART. It enables to configure the recorder, to create directory, to create files, to read number of directory and files already written on disks, to read the available disks space, to read a sector of a disk, etc… and run the recording or the reading of disks. Please have a look on the Demo Data Sheet to have a complete list of the available menu.

Some example of configurations:

Configuration	Resources needed		Remarks
1 DDR_FIFO RAID0 - 1 SATA IP	FF: 22K LUT: 27K Memory LUT: 2K GT: 1	BRAM: 171 BUFG : 11 MMCM: 3 PLL: 1	None
1 DDR_FIFO RAID0 - 2 SATA IP	FF: 26K LUT: 30K Memory LUT: 2.1K GT: 2	BRAM: 183 BUFG : 11 MMCM: 3 PLL: 1	Bandwidth limited by DDR FIFO in case of Gen3
2 DDR_FIFO RAID0 - 2 SATA IP	FF: 27K LUT: 31K Memory LUT: 2.1K GT: 2	BRAM: 189 BUFG : 11 MMCM: 3 PLL: 1	Bandwidth limited by DDR FIFO in case of Gen3
2 DDR_FIFO RAID0 - 4 SATA IP	FF: 35K LUT: 40K Memory LUT: 2.5K GT: 4	BRAM: 212 BUFG : 11 MMCM: 3 PLL: 1	Bandwidth limited by DDR FIFO in case of Gen3

Other configurations are possible according to user needs, please feel free to ask us.

General Description

The LDS_SATA_RECORDER_XA7 IP is a complete recording system IP. It can be configured according to the recording performance required and the quantity of the data to record. The LDS_SATA_RECORDER_XA7 IP is available only on Xilinx Artix 7 FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Related Information

Logic Design Solutions

106 Boulevard de la Résistance
93460 Gournay sur Marne – France.
Phone : +33 (0) 1 45 92 24 47
E-mail : info@logic-design-solutions.com
WEB: http://www.logic-design-solutions.com