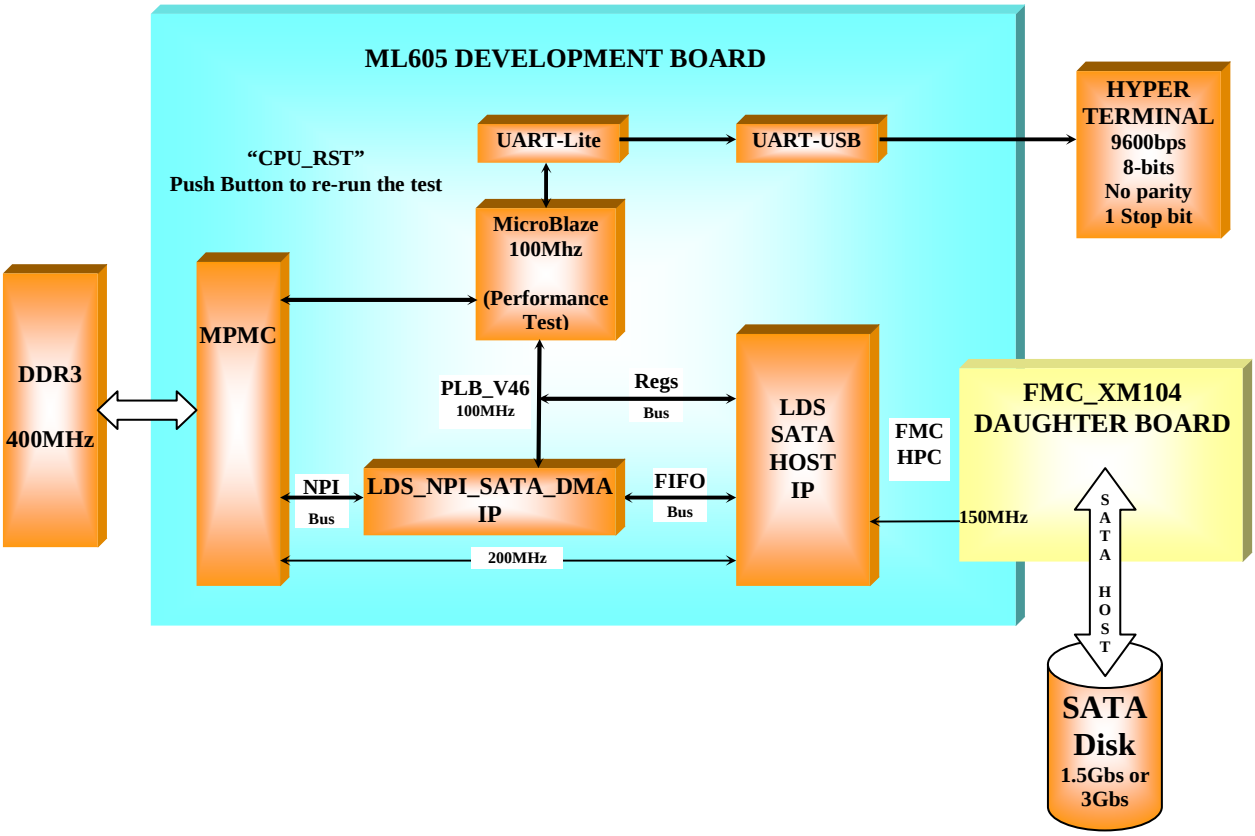
# Virtex 6 SATA Host Controller
## *IP*

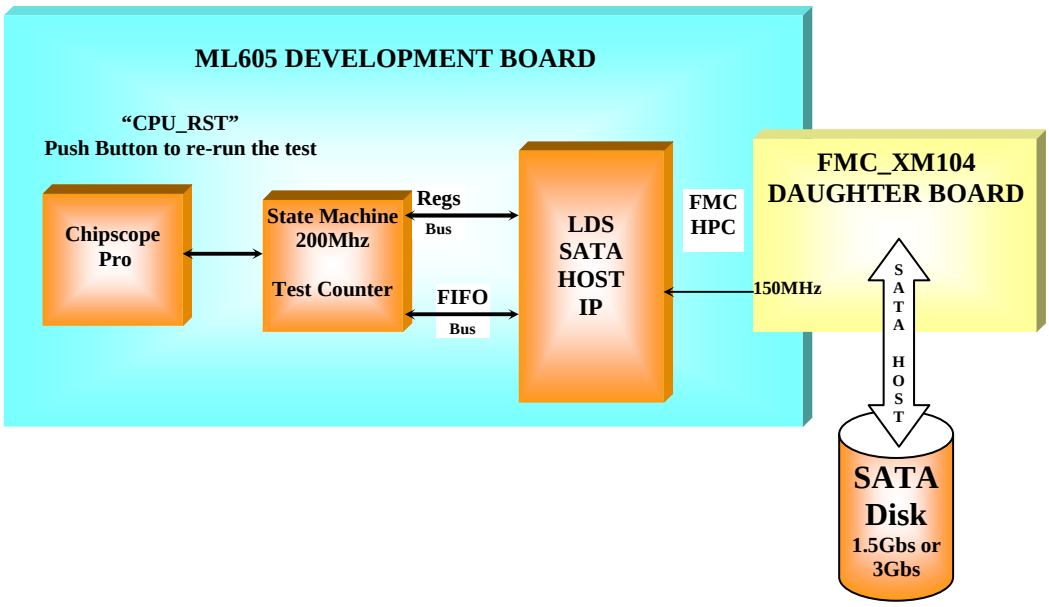
## Product Brief

Nov. 10 – Ver. 1.0

### MicroBlaze Demo provided under NDA




### State Machine Demo provided under NDA



# Features

The LDS_SATA_HOST_XV6 IP incorporates the Transport layer, the Link layer and the PHY layer on a Xilinx Virtex 6 FPGA. The LDS_SATA_HOST_XV6 IP is compliant with Serial ATA II specification and signaling rate is 1.5Gbps and scalable 3Gbs (*6Gbs under way*). The LDS_SATA_HOST_XV6 IP is fully synchronous with system frequency (Clock_sys) at 37.5MHz in case of 1.5Gbps speed selection and 75MHz in case of 3Gbs speed selection. The source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.

### Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provides a 16 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in Xilinx Virtex 6 GTX Macro
- **Automatic Speed negotiation 1.5Gbs or 3Gbs**

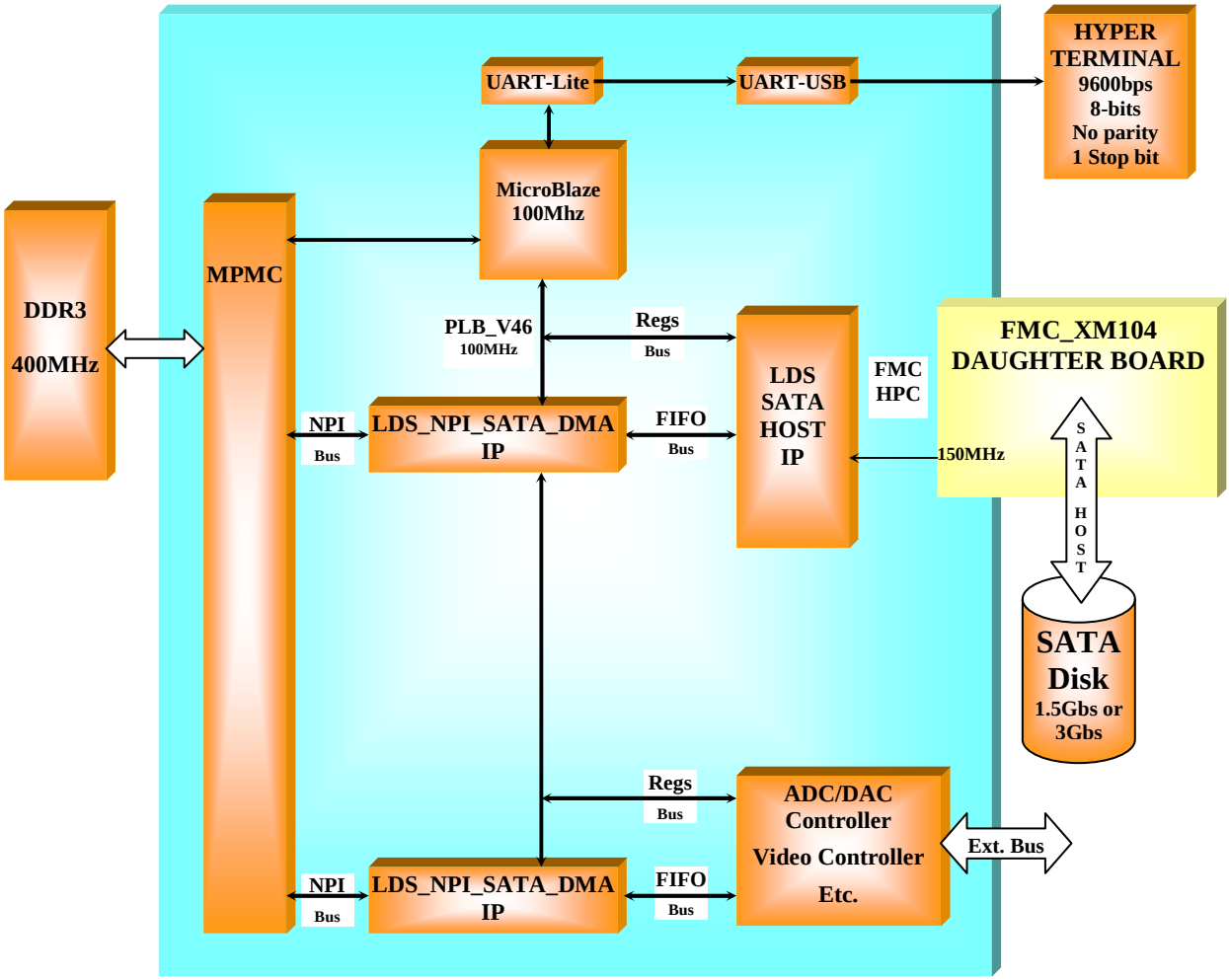
### Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- The interface between the link layer and the transport layer is 32-bit wide

### Transport Layer features

- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs (FIFO interface provided)
- Support DMA Abort primitive

## Application Example




## Verification

The LDS-SATA_HOST_XV6 IP has been validated on the Xilinx ML605 DEVELOPMENT BOARD and several hard drives.

## Performance

The demo provided on the Xilinx ML605 DEVELOPMENT BOARD makes a Disk Read and Write performance test on each disk connected. A counter value is written on the disk and then read back.

Example : Intel X25 SSD 3Gbs => 1Gbytes transfer at 200MB/s in sequential read and write – DMA transfer of 128 sectors.

## Design Package

| | |
|---|---|
| **Device Family** | **Xilinx Virtex 6 LXT FPGA**<br>**speed grade : 1 (up to 3Gbs)**<br>**speed grade : 2 (up to 6Gbs)** |
| **Number of occupied Slices** | 1000 (IP core only) |
| **Package file** | **Synthesis Netlist :** Data Sheet and Constraint File |
| | **Source code :** Data Sheet, SATA EDK project Description,<br>PLB SATA HOST Interface Description and Constraint File. |
| **Design Tool Used** | Xilinx XST VHDL synthesis.<br>ModelSim simulation tool from ModelTech.<br>Xilinx ISE Place and Route software. |
| **Support** | Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available. |

## General Description

The LDS_SATA_HOST_XV6 IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA_HOST_XV6 IP is available only on Xilinx Virtex 6 LXT FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

## Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

## Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.


## Available Support Products

Support products available from Logic Design Solutions.

## Related Information

### Logic Design Solutions

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