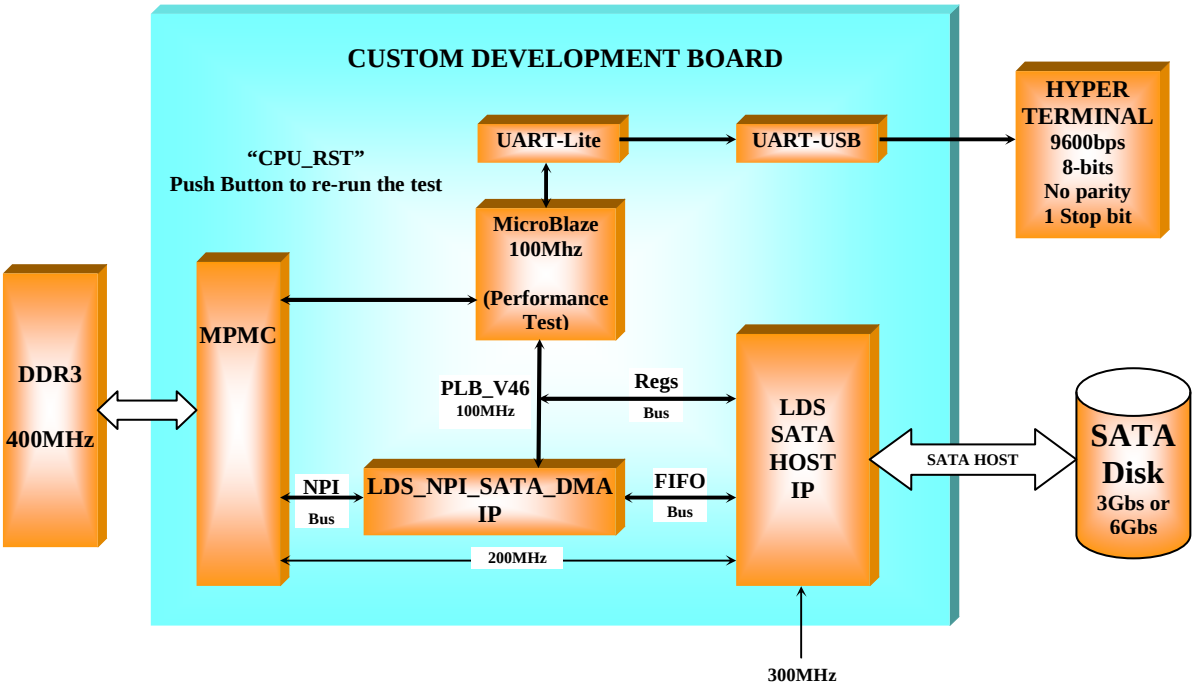
Virtex 6 SATA 3 Host Controller
IP

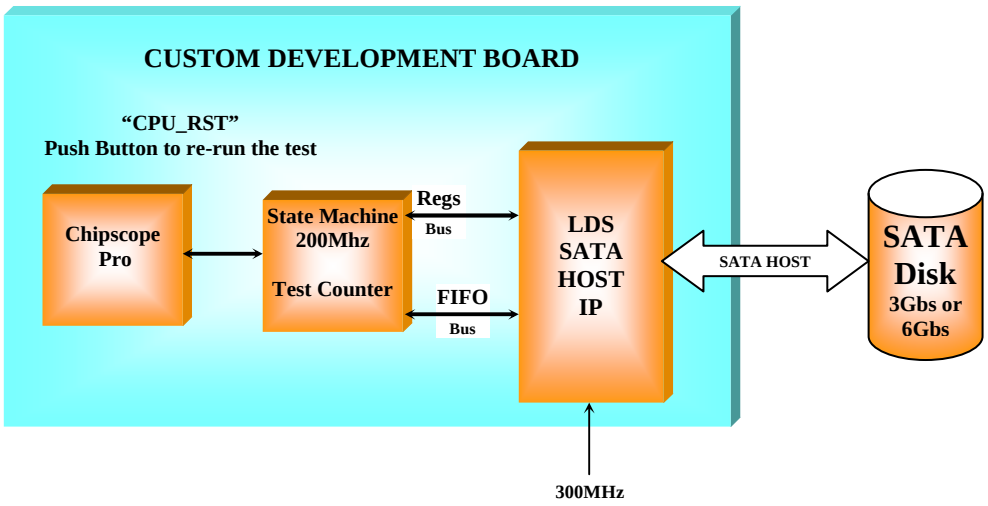
Product Brief

February. 12 – Ver. 1.0

MicroBlaze Demo provided under NDA



State Machine Demo provided under NDA



Features

The LDS_SATA3_HOST_XV6 IP incorporates the Transport layer, the Link layer and the PHY layer on a Xilinx Virtex 6 speed grade 2 FPGA. The LDS_SATA3_HOST_XV6 IP is compliant with Serial ATA III specification and signaling rate is 1.5Gbps and scalable 6Gbs. The LDS_SATA3_HOST_XV6 IP is fully synchronous with system frequency (Clock_sys) at 37.5MHz in case of 1.5Gbps speed selection and 75MHz in case of 3Gbs speed selection and 150MHz in case of 6Gbs speed selection. The source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.

Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provides a 16 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in Xilinx Virtex 6 GTX Macro
- **Automatic Speed negotiation 3Gbs or 6Gbs**

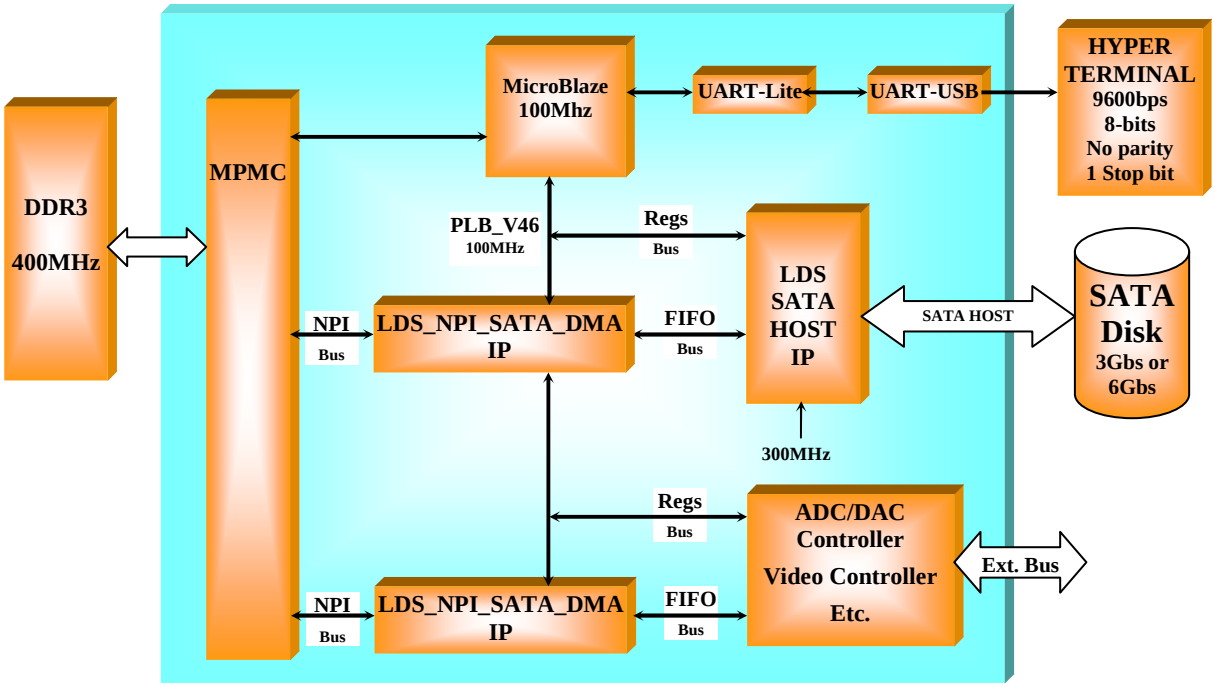
Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- CONT primitive management in receive and transmit
- The interface between the link layer and the transport layer is 32-bit wide

Transport Layer features

- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs (FIFO interface provided)
- Support DMA Abort primitive
- NCQ Support.

Application Example



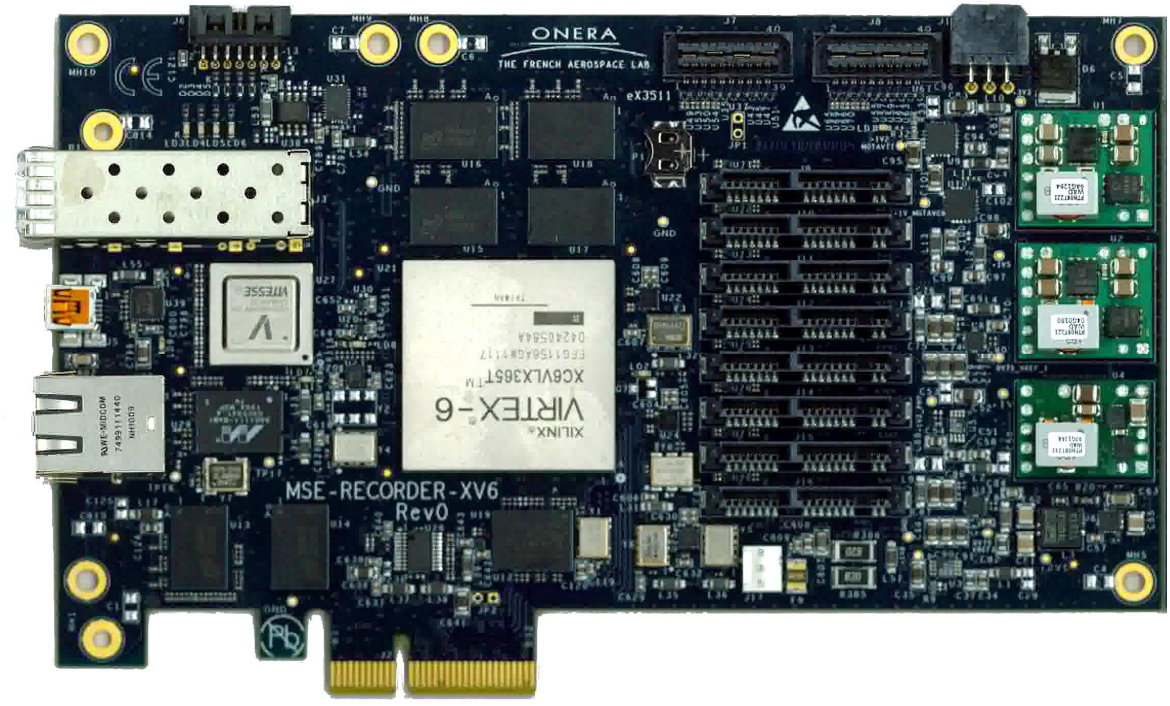
Verification

The LDS_SATA3_HOST_XV6 IP has been validated on a Custom BOARD : **MSE-RECORDER-XV6.** This board has been designed for ONERA 'THE FRENCH AEROSPACE LAB' by ESTAR Company.

ONERA
THE FRENCH AEROSPACE LAB

ESTAR

You can buy the **MSE-RECORDER-XV6** Board through Logic Design Solutions.



MSE-RECORDER-XV6 Board Features :

- FPGA Xilinx Virtex-6 LX365T -2 or -3
- 8 x SATA III (6Gb/s)
- Ethernet 10G SFP + and 1G
- 1.5GB DDR3 - 533MHz
- 2 x SAMTEC QSH (43.2Gb/s perc connector)

Performance

The demo provided on the Custom BOARD makes a Disk Read and Write performance test on each disk connected. A counter value is written on the disk and then read back.
Example : Intel SSD 510 Series 6Gbs => 50Gbytes transfer at 270MB/s in sequential write and 350MB/s in sequential read – DMA transfer of 256 sectors.

Design Package

Device Family	**Xilinx Virtex 6 LXT FPGA** **speed grade : 2**
Number of occupied Slices	1000 (IP core only)
Package file	**Synthesis Netlist :** Data Sheet and Constraint File
	Source code : Data Sheet, SATA EDK project Description, PLB SATA HOST Interface Description and Constraint File.
Design Tool Used	Xilinx XST VHDL synthesis. ModelSim simulation tool from ModelTech. Xilinx ISE Place and Route software.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

General Description

The LDS_SATA3_HOST_XV6 IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA3_HOST_XV6 IP is available only on Xilinx Virtex 6 LXT FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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