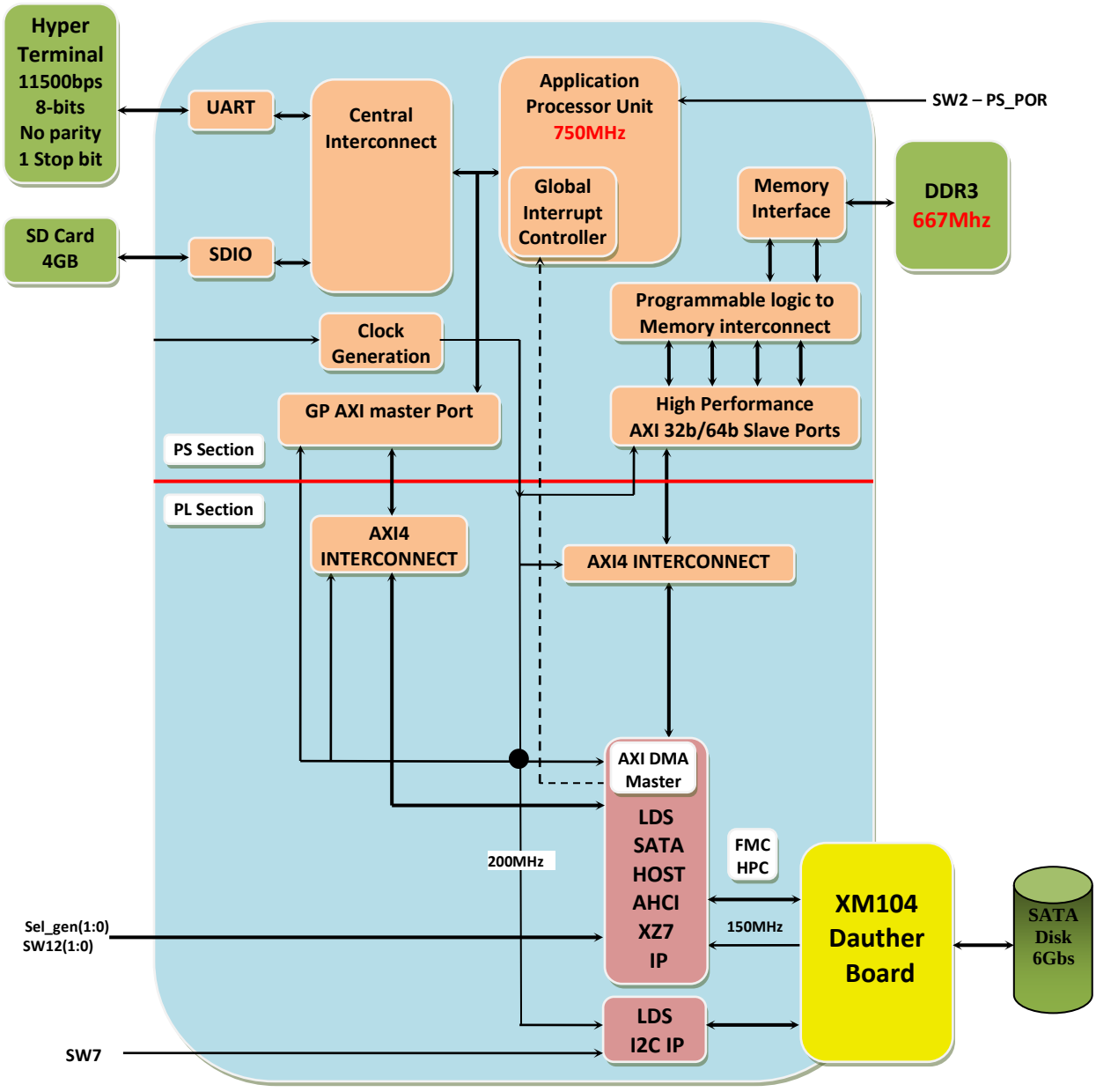
ZYNQ SATA 3 AHCI Host Controller *IP* with Linux Driver

Product Brief

Jun 16 – Ver. 1.0

ZC706 + XM104 Demo provided under NDA with Linux Driver



- The ZC706 board must be configured to boot on the SD Card with the switch SW16 set.
- The Linux Driver and the BSP have been done by Armadeus Systems : www.armadeus.com
- At power up Linux starts automatically.
- You can use 'root' for the login and the password.
- Then you can use the disk.
- Reliability and Performance shell test are provided
- Please have a look on the demo data sheet to get details about the demo.
- Sel_gen(1:0) switch enables to choose between Gen3 (11\b) and Gen2 (10\b) SATA speed. The Sel_gen(1:0) value must always be set to Gen3 (11\b) during FPGA configuration. When FPGA configuration is done, the speed can be switch to Gen2.

Features

The LDS_SATA3_HOST_AHCI_XZ7 IP incorporates the AHCI registers model, the Transport layer, the Link layer and the PHY layer on a Xilinx Zynq speed grade 2 FPGA. The LDS_SATA3_HOST_AHCI_XZ7 IP is compliant with Serial ATA III specification and signaling rate is 6Gbs. The LDS_SATA3_HOST_AHCI_XZ7 IP is fully synchronous with system frequency (Clock_sys) at 75MHz in case of 3Gbs speed selection and 150MHz in case of 6Gbs speed selection. The source code format is available for ease of customization. The customization can be done by Logic Design Solutions.

Linux Driver features

- Linux Kernel 4.0 patch adding SATA/AHCI for LDS_SATA3_HOST_AHCI_XZ7 IP
- Linux AHCI SATA Driver compatible
- Provide standard Linux block device interface
- Easy to adapt to the future version of Linux Kernel
- Support any Linux file system
- Linux Kernel 4.0 – tested and validated with kernel 4.0 from Xilinx
- Linux open firmware / device tree
- Linux standard device interfaces

AHCI features

- 1 port
- AHCI Generic Host Registers set
- AHCI Port Host Registers set

Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provides a 32 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in Xilinx Zynq GTX Macro
- 6Gbs or 3Gbs Speed

Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- CONT primitive management in receive and transmit

Transport Layer features

- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs (FIFO interface provided)
- NCQ Support.

Verification

The LDS_SATA3_HOST_AHCI_XZ7 IP has been validated on the ZC706 + XM104 evaluation Board and several disks. List of disk available on request.

IP Package

Device Family	**Xilinx ZYNQ FPGA** **speed grade : 1/2**
Number of occupied Slices	2000 (IP core only)
SATA IP Package file	**Source code or Synthesis Netlist :** Data Sheet, VIVADO Project, SATA HOST AHCI AXI Interface Description and Constraint File.
Linux Package	**Linux package has been done** by Armadeus Systems : www.armadeus.com **Linux demo bootable SD card**: - compatibles with ZC706+XM104 boards - linux kernel 3.12 with AHCI/SATA driver - provides standard Linux block device interface - Based on linux Ubuntu for ARM Linux demo user manual **Linux kernel 4.0 Zynq AHCI patch:** - adds driver compatibility with AHCI/SATA for the ZC706+XM104 evaluation boards - adds device tree compatibility with AHCI/SATA for the ZC706+XM104 evaluation boards - easy to adapt to the future version of Linux kernel - compatible with any linux filesystem supporting the AHCI/SATA standards **Linux kernel 4.0 Zynq AHCI documentation:** - provides instruction to apply the linux patch - provides information and procedures to support other customer boards and/or Linux kernel version Patch is provided under open source license GPL V2. **Options :** **Support of Linux kernel other than 4.0** **Support of Xilinx BSP**
Design Tool	Xilinx VIVADO 2015.4
IP Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.
Linux Support	**6 months/24H phone email support** Support is provided by Armadeus Systems : www.armadeus.com through LDS.

General Description

The LDS_SATA3_HOST_AHCI_XZ7 IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA3_HOST_AHCI_XZ7 IP is available only on Xilinx ZYNQ FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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