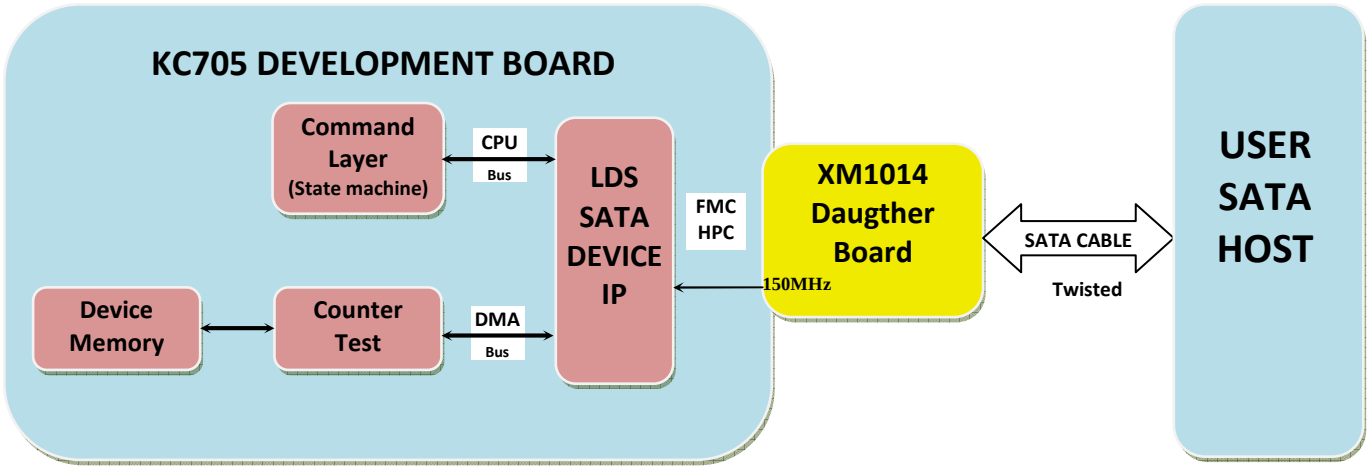
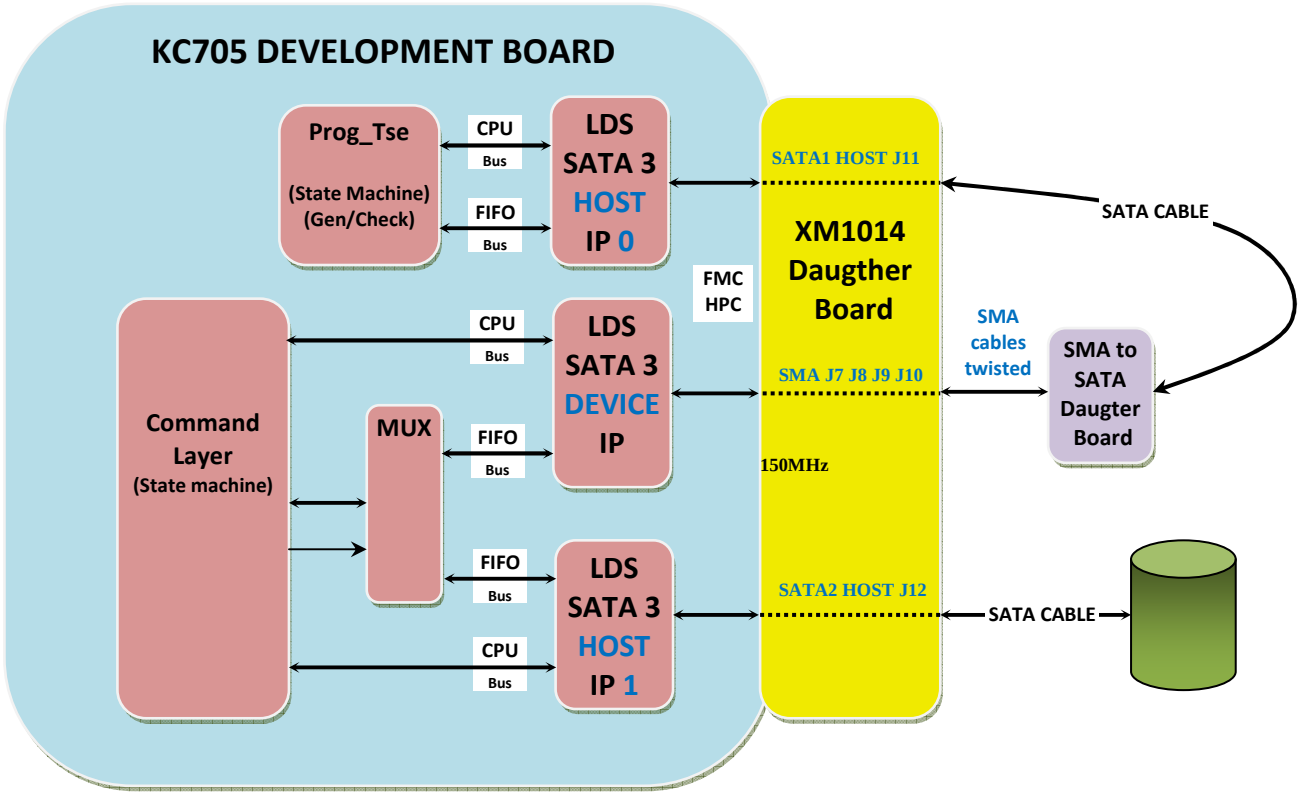
Kintex 7 SATA III DEVICE Controller
IP

Product Brief
January 14 – Ver. 1.0

Demo 1 provided under NDA



Demo 2 provided under NDA



Features

The LDS_SATA3_DEVICE_XK7 IP incorporates the Command Layer, Transport layer, the Link layer and the PHY layer on a Xilinx Kintex 7 FPGA. The LDS_SATA_DEVICE_XK7 IP is compliant with Serial ATA III specification and signaling rate is 3Gbps and scalable 6Gbs. The LDS_SATA_DEVICE_XK7 IP is fully synchronous with system frequency (Clock_sys) at 75MHz in case of 3Gbps speed selection and 150MHz in case of 6Gbs speed selection. The source code format is available for ease of customization. Ie can be customized by Logic Design Solutions and **DO254** documentation is available on request.

Physical Layer features

- Detect OOB and COMWAKE
- Detect the K28.5 comma character and provides a 32 bit parallel output
- Power management mode handled by state machine (shared between Phy and Link layer)
- Provides error indication to upper layers
- 8b/10b encoding and decoding in Xilinx Kintex 7 GTX Macro
- Manual Speed selection 3Gbs or 6Gbs

Link Layer features

- Scrambling of tx data and descrambling of rx data
- CRC 32 calculation and check
- Report transmission status and error to Transport Layer
- Enable BIST loopback and pattern generation modes
- Auto inserted hold primitive to avoid FIFO overflow and underflow
- Partial and slumber power management modes
- The interface between the link layer and the transport layer is 32-bit wide

Transport Layer features

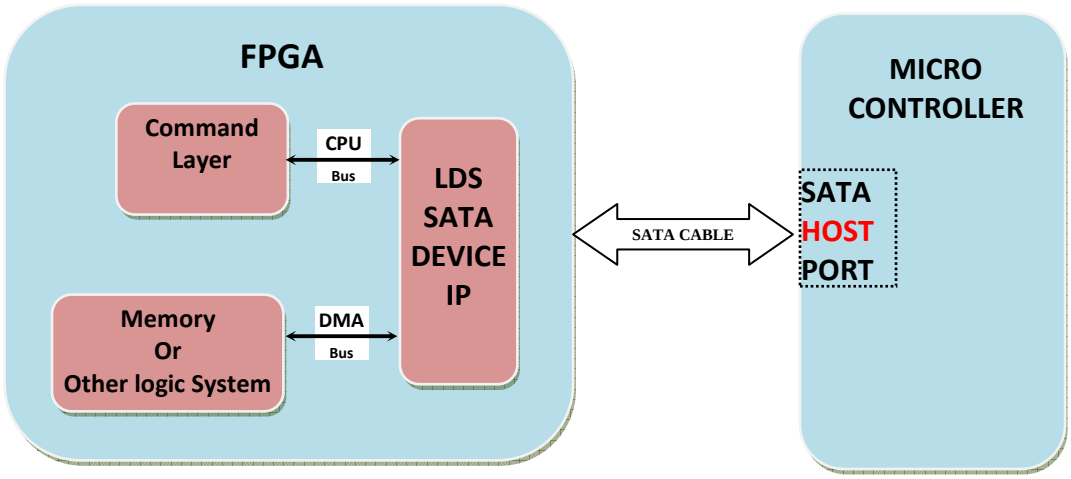
- 48-bits sector address
- Programmed IO (PIO) and DMA modes
- Support BIST FIS transmission and reception
- Automatic error FIS retry capability
- Implement Shadow Registers and SATA SuperSet registers
- Simple synchronous CPU and DMA Interface for data transfers including DMA hold-off capability
- DMA interface can be connected easily to memory space or FIFOs (FIFO interface provided)
- Support DMA Abort primitive

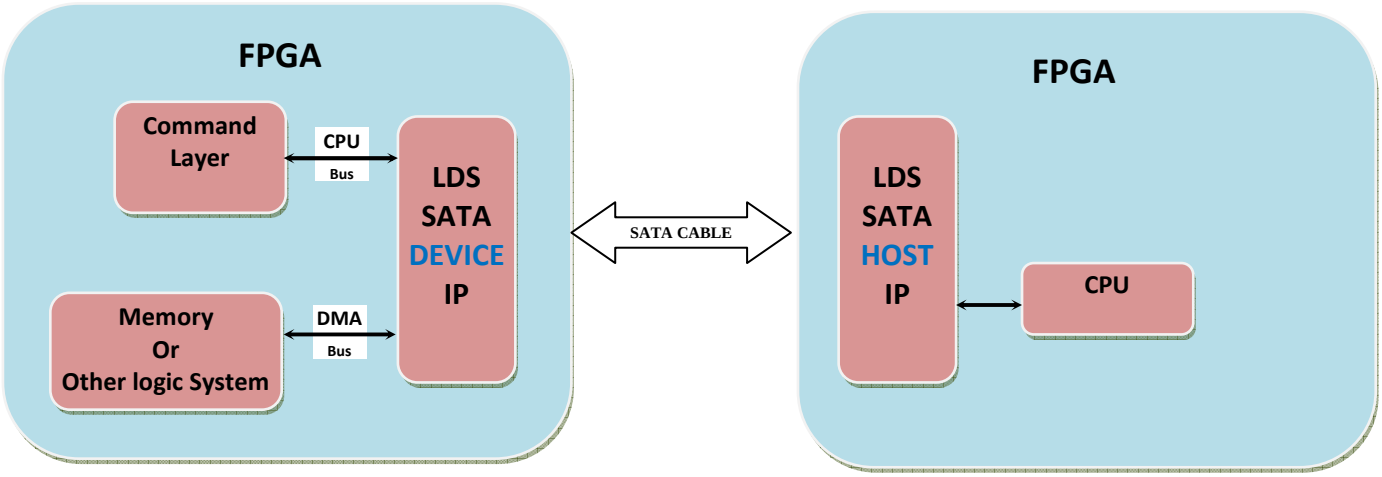
Command Layer features

- The Command Layer is always provided in Source code.
- The customer is able to modify the command layer.
- The Command layer is managing by default :
    - IDENTIFY DEVICE
    - IDLE (NON DATA Protocol)
    - READ_SECTOR_EXT (PIO-IN Protocol)
    - WRITE_SECTOR_EXT (PIO-OUT Protocol)
    - READ_DMA_EXT (DMA IN Protocol)
    - WRITE_DMA_EXT (DMA OUT Protocol)
    - SOFTWARE RESET Protocol
    - HARDWARE RESET Protocol

Application Example

The SATA Standard can be used to transfer data between a Microcontroller and a FPGA, or from a FPGA to another FPGA.





Verification

The LDS_SATA3_DEVICE_XK7 IP has been validated on the Xilinx KC705 DEVELOPMENT BOARD.

Performance

The LDS_SATA3_HOST IP has been connected to the LDS_SATA3_DEVICE IP.
A 500Gbytes transfer is done at 540MB/s in sequential write and 560MB/s in sequential read – DMA transfer of 2048 sectors.

Design Package

Device Family	**Xilinx Kintex 7 LXT FPGA** **speed grade : 2**
Number of occupied Slices	1000 (IP core only)
Package file	**Netlist or VHDL Source code :** Data Sheet and Constraint File.
Design Tool Used	Xilinx XST VHDL synthesis. ModelSim simulation tool from ModelTech. Xilinx ISE -VIVADO 2012.4. - Place and Route software.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contracts available.

General Description

The LDS_SATA3_DEVICE_XK7 IP implements a single-chip synchronous Serial-ATA macro which can be used to interface between memory and Serial-ATA devices. The LDS_SATA3_DEVICE_XK7 IP is available only on Xilinx Kintex 7 LXT FPGA.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Recommended Design Experience

Designers should be familiar with Serial ATA, VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The IP can be easily integrated into hierarchical VHDL designs.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

Logic Design Solutions
106 Boulevard de la Résistance
93460 Gournay sur Marne – France.
Phone : +33 1 45 92 24 47
E-mail : info@logic-design-solutions.com
WEB: http://www.logic-design-solutions.com